Appeal No. 2014-1508

United States Court of Appeals

for the

Federal Circuit

EMCORE CORPORATION,

Appellant,

– v. –

NICHIA CORPORATION,

Appellee,

– and –

MICHELLE K. LEE, Deputy Under Secretary of Commerce for Intellectual Property and Deputy Director of the U.S. Patent and Trademark Office,

Intervenor.

APPEAL FROM THE UNITED STATES PATENT AND TRADEMARK OFFICE, PATENT TRIAL AND APPEAL BOARD IN NO. IPR2012-00005

OPENING BRIEF FOR APPELLANT

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August 27, 2014

CERTIFICATE OF INTEREST

Counsel for Appellant Emcore Corp. certifies the following:

1. The full name of every party or amicus represented by me is:

   Emcore Corp.

2. The name of the real party in interest (if the party named in the caption is not the real party in interest) represented by me is:

   Emcore Corp.

   Everlight Electronics Co., Ltd.

3. All parent corporations and any publicly held companies that own 10 percent or more of the stock of the party or amicus curiae represented by me are:

   N/A

4. The names of all law firms and the partners or associates that appeared for the party or amicus now represented by me in the trial court or agency or are expected to appear in this court are:

   Winston & Strawn LLP: Michael Tomasulo, Michael Scheer, Geoffrey Eaton, David Lin, and Eric Werlinger

Dated: August 27, 2014

/s/ Geoffrey P. Eaton
Geoffrey P. Eaton

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STATEMENT OF RELATED CASES

No other appeal in or from this action is or was previously before this or any other appellate court. Counsel is aware of no cases pending in this or any other court that will directly affect or be directly affected by the Court's decision in this appeal.

JURISDICTION

The Patent Trial and Appeal Board had jurisdiction pursuant to 35 U.S.C. §§6(b)(4) and 316(c). The Board's Final Written Decision issued on February 11, 2014, and the Notice of Appeal was timely filed on April 15, 2014. This Court has jurisdiction over the appeal pursuant to 35 U.S.C. §141(c) and 28 U.S.C. §1295(a)(4)(A).

ISSUES PRESENTED

In this inter partes review proceeding, the Patent Trials and Appeals Board found the '215 patent invalid as obvious over various combinations of at least five prior art references. The issues presented are:

1. Where the disclosed purpose of the invention is the creation specifically of *low*-resistance semiconductor contacts, did the Board err by construing the claim terms "annealing" and "base layer" so broadly that the claims would cover *high*-resistance contacts?

2. Under any claim construction—and especially the correct one—is the Board's judgment of invalidity for obviousness supported by substantial evidence, where:

    a. One of the primary prior art references on which the Board relied to invalidate the challenged claims was not identified in or submitted

with Nichia's IPR petition, as expressly required by 35 U.S.C. §312(a)(3)?

b. None of the admissible prior art references teaches a causal relationship between annealing a semiconductor contact and a decrease in contact resistance?

c. All of the admissible prior art references teach that annealing a contact with an aluminum base layer and a gold top layer will result in degradation of the gold layer, and so teach away from the use of the claimed aluminum base layer?

3. Under any claim constructions, did the Board err in finding the '215 patent invalid for obviousness without articulating any motivation to combine the prior art references?

BACKGROUND

The '215 patent relates to semiconductors, and specifically to a method of fabricating contacts for n-type semiconductors for use in light-emitting diodes ("LEDs"). Understanding the Board's decision and the errors that compel its reversal requires a brief explanation of semiconductors and contacts, their function in LEDs, the identification in the prior art of a particular problem in existing methods of fabricating LED semiconductor contacts, and the '215 patent's solution to that problem.

I. Technical Background: Semiconductors and LEDs

A. Semiconductors and Contacts

A semiconductor, as its name suggests, is a material that conducts electricity at a level less than that of a true conductor (like copper) and more than that of an insulator (like glass). A "GaN" semiconductor is one made up of gallium nitride, a material widely used in fabricating LEDs.

Semiconductors offer conductive properties that make them particularly useful in electrical circuits—properties like variable resistance, the ability to conduct current more efficiently in one direction than another, and sensitivity to heat and light. Their conductive properties can be manipulated in a variety of ways, from introducing greater or lesser quantities of impurities (i.e., other materials), to heating, to exposure to a magnetic field.

A semiconductor "contact" is a structure that connects a power source to a semiconductor and passes electrical current to it. Regions of a semiconductor having n-type conductivity ("n-GaN") and regions having p-type conductivity ("p-GaN") employ n-contacts and p-contacts, respectively.[1] The interaction between p-contacts and n-contacts is what allows LEDs to make light: "When an electrical voltage is applied between" the contacts from a power source, "electrons in the n-type region and holes in the p-type region move toward the junction and combine with one another at or adjacent to the junction to produce light." A00133.

The efficiency with which current passes through the contact is expressed in terms of "resistance." In the context of LEDs, low resistance is generally desirable: "a light emitting diode with low resistance ohmic contacts can convert electrical power into light more efficiently than a similar diode with high resistance contacts." A00133.

Finally, LED contacts are "typically" connected to "metallic leads as, for example, by wire-bonding processes." A00133. The metallic leads (or wires) connect the contact to a power source. When the contact is in use, current flows from the power source through the wires, through the contact, and into the semiconductor material.

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[1] In *n-type* conductivity, electrical current is carried principally by electrons. In *p-type* conductivity, electrical current is carried principally by electron vacancies, commonly referred to as "holes." A00133. The invention of the '215 patent relates to n-GaN contacts.

B. Semiconductor Devices and LEDs

Broadly speaking, an LED is a semiconductor device that emits light when electrical energy is applied and an electrical current flows through the semiconductor material. Based on the semiconductor material, an LED can be designed to emit a specific type of light, e.g., infrared, ultraviolet, or any color in the visible spectrum. A00333.

To emit light, an LED requires that a current be conducted through a semiconductor p-n junction. The current is supplied by some power source, such as a battery. Power from this source can be conducted through metal wires to the LED. The wires are attached to the LED at contact points, typically comprised of a metal layer or metal layers. The current is passed to the n-type semiconductor through the n-type contact. A00334-35.

The overall efficiency of the LED is significantly affected by how efficiently the charge carriers can be injected to the p-n junction. Part of the efficiency associated with the injection process is how efficiently electricity is introduced from the power supply into the semiconductor through its contacts. Lower contact resistances improve the overall device performance in this way. A00335-36.

Rapid development in LED technology began in the 1980s and 1990s because of significant developments in gallium arsenide (GaAs) and GaN semiconductor technology. In the 1980s, GaAs-based LEDs were significantly

improved to be more efficient and brighter, enabling their use in a wide range of applications. In the early 1990s, research by Dr. Shuji Nakamura led to the first commercially viable GaN-based LED. GaN-based LEDs quickly became a primary focus of LED research because of their ability to emit green, blue, or ultraviolet light. With the introduction of blue LEDs, it also became possible to produce white light, the "holy grail" of LED technology. A00333-34.

Since then, each component of a GaN-based LED, including the contacts, has been the subject of intense research in order to improve performance and reduce costs. Developments in the processing of n-type contacts have played an important role in improving GaN-based LEDs. Despite this drive, even in 1997, six years after the development of the GaN-based LED, there was still a dearth of information regarding the interaction of a contact's metal layers and a GaN semiconductor. A00334.

II. Properties Of LED Semiconductor Contacts

To perform effectively in an LED device, a semiconductor contact should feature three qualities. First, the contact should be ohmic and have a *low contact resistance*; that is, it should convert power into light as efficiently as possible. Second, the contact should be *thermally stable*. Third, the contact should offer *reliable wire bonding*. A00336-38.

A. The Importance Of Low Contact Resistance

A purpose of an ohmic contact is to allow electric current to pass into and out of an LED with a minimum amount of resistance. The more resistance to the flow of electricity provided by the contact, the more energy it will take for an electric current to pass through the contact. If additional energy is consumed at the contact, heat will be generated, which is deleterious to the operation of the device. A00338-39. As Nichia's expert explained, at the time of the invention, anything greater than 10^{-5} Ωcm^2 would have been considered "poor" contact resistance, making the contact a "poor contact." A00157.

B. The Importance Of Thermal Stability

Thermal stability is another important quality in an LED contact. Depending on the type of device, the semiconductor and/or the contact can become quite hot during operation, which can damage a contact that is not thermally stable. Then, the contact cools to room temperature when not in operation. Heating and cooling cycles can also have deleterious effects on a semiconductor or contact. It is important that the contact be able to withstand these heating and cooling cycles. A00339.

C. The Importance Of Reliable Wire Bonding.

Finally, an effective LED contact should bond well with the electrical current source. Thus, the top layer should adhere well to the current source

(frequently but not always a metal wire), be highly conductive, soft (to accommodate thermal expansion), and sufficiently thick in order to reduce the possibility of cratering during bonding. A good surface morphology for the top layer is important – it allows for consistent bonding to wires and other current sources. Poor surface morphology can lead to device failure. A00340.

III. The Problem To Be Solved: Combining An Aluminum Base Layer, A Gold Top Layer, And An Annealing Step To Create A Contact Featuring Both Low Resistance And Reliable Wire Bonding.

All the desirable qualities of an LED semiconductor contact are affected by the materials used in the contact, the order in which they are layered, and other variables such as the introduction of heat via an annealing process. As Nichia itself has conceded, "the selection of a particular material combination for providing metal-semiconductor contacts is not a simple choice of equivalent alternatives but rather the result of detailed investigations of the complex and technical interactions between the metal and semiconductor materials." A00396-97. The complex interactions between the contact materials, the semiconductor materials, the current source, and other variables make it difficult to construct contacts that excel in all three key qualities—contact resistance, thermal stability, and reliable bonding.

For example, scientists have experimented with aluminum as a base layer in light of its inherent reflective properties. A00352-53. Similarly, gold has been

tested as a potential top layer. But for many years, those materials could not be used together in the same contact, because when subjected to heat, the metals interact in ways that "impair the reliability of the wire bonds." A00133. Numerous prior art references disclose the industry's continuing inability to fabricate an LED contact that employs both an aluminum base layer and a gold top layer, while still achieving both low contact resistance and reliable wire bonding. These issues were never satisfactorily resolved—until the invention of the '215 patent.

IV. The Industry Tried For Years To Fabricate An Effective LED Contact Using Aluminum As A Base Layer.

As explained below, Nichia's own references demonstrate that from 1992 onward, Nichia and many others tried and failed to use Al as a base layer to n-type GaN, finding that it either increased contact resistance, degraded wire bonding, or both.

A. 1993: Nichia And Dr. Nakamura Experiment With Al As A Base Layer And Conclude That It Unacceptably Degrades When Annealed And Impairs Wire Bonding.

Nichia and Dr. Nakamura's early research into contacts for n-type GaN focused on aluminum and indium. These efforts failed, because the use of aluminum as the contact layer caused problems with both the contact's conductivity and its wire bonding. Nakamura's patent states this emphatically:

> [I]t has been found that **aluminum** and indium can hardly establish an ohmic contact with the n-type gallium nitride-based III-V Group compound semiconductor layer, **and tend to degrade by an annealing treatment, losing the electrical conductivity.**
>
> A00208.

Nakamura also concluded that Al was a poor base layer for n-type GaN because it led to poor bonding with the current source. A00215.

By 1996, when Nakamura issued, the industry was acutely aware that then-industry leaders Nichia and Dr. Nakamura had concluded that Al did not form good ohmic contacts with n-type GaN and tended to degrade on annealing. A00343. For that reason, Dr. Nakamura considered Ti to be the preferred base layer for n-type GaN. *See* A00215; A00343.

B. 1993: Foresi Finds That Al Base Layers Show Poor Contact Resistance, Which Increased On Annealing.

In 1993, Foresi experimented with Al as a base layer to n-type GaN. Foresi & Moustakas, A00243-45 Not only did the resulting contacts have poor contact resistance (10^{-3} Ωcm^2 to 10^{-4} Ωcm^2) by Nichia's own standards, A00157, the experiment showed that the contact resistance of the Al-based contact *increased upon annealing*, suggesting that aluminum would not be an effective choice for the base layer in a low-resistance LED contact. A00344-46.

C. 1995-1997: Shibata Reports Successful Use Of An Al Base Layer, But Industry Leader Toshiba Is Unable To Replicate Shibata's Results.

In 1995, an unexamined Japanese patent application included a short disclosure directed to the use of an n-GaN contact employing an aluminum base layer, a titanium barrier layer, and a gold top layer. A00236. Shibata reported that this structure successfully created an ohmic contact with good wire bonding and contact resistance "of 10^{-5} Ωcm or less." A00241. The latter disclosure is ambiguous: the correct unit of measure for contact resistance is not Ωcm, but Ωcm^2. Even if (as Nichia has argued) this is merely a typographical error, it calls into question the accuracy of the disclosure. A00341-49.

If the Shibata disclosure were accurate, it would have represented a major breakthrough in LED contact fabrication. But the evidence strongly indicates that Shibata's disclosure was unreliable. Less than two years after Shibata, Dr. Fujimoto—working for one of the world leaders in semiconductor fabrication, Toshiba Corporation—repeated Shibata's testing and conducted a significant amount of additional experimentation directed to making a low-resistance, ohmic contact to n-type GaN using an Al base layer. Fujimoto later reported that he was *unable to replicate* Shibata's results. A00185. Instead, consistent with all the pre-Shibata prior art, Fujimoto found that Shibata's Al/Ti/Au contact "invited an *increase* in contact resistance of the electrode" and "degrade[d] wire bonding" in the Au top layer. A00185. Accordingly, Fujimoto concluded that contrary to

Shibata's disclosure, the problem of "deterioration or decomposition" when using an Al base layer with an Au top layer "still remains unsolved." A00185.

D. 2000: The Admitted Prior Art Shows That Problems With Al Base Layers Persist.

By 2000, in the background section of a provisional application, the inventors of the '215 patent reported that those problems still remained unsolved. A00172; A00351-52. Particularly, the background of the provisional states that annealing contacts with an Al base layer is "accompanied by degradation in the surface morphology, due to metallurgical reactions between the metal layers in the stack." A00172. Nichia's expert described this as a "warning" that annealing an Al-based contact could lead to "degradation" of the device. A00701-02.

V. The '215 Patent Solves The Problems With Al Base Layers.

The inventors filed the application that became the '215 patent on October 5, 2001. The Abstract describes the invention succinctly:

> A contact for n-type III-V semiconductor such as GaN . . . is formed by depositing Al, Ti, Pt, and Au in that order on the n-type semiconductor and annealing the resulting stack, desirably at about 400-600 C, for about 1-10 minutes. The resulting contact provides a low-resistance, ohmic contact to the semiconductor and excellent bonding to gold leads.
>
> A00130.

That is, the invention employs an aluminum base layer; two intervening layers made of titanium and platinum; and a gold top layer. It then anneals the

stack. The resulting contact, unlike prior art Al/Au contacts, features *both* low resistance *and* good wire bonding. One key to the patent's breakthrough is the use of multiple barrier layers composed of titanium and platinum. The barrier layers act to "prevent undesirable reactions between Al and the metal of the top layer Au during annealing." A00133. Unlike prior art efforts to use barrier layers, however, the invention's Ti and Pt barrier layers do not unacceptably increase contact resistance. A00133.

A. The Invention Achieves Low Resistance, Thermal Stability, And Reliable Wire Bonding In An Al-Based Contact.

1. The contact has a low contact resistance.

The '215 patent discloses a contact with an Al base layer that has a contact resistance "of the order of 10^{-5} ohm-cm^2 or lower," A00134; A00383-84, which Nichia's expert characterizes as a "good" contact resistance for the time. A00157.

2. The contact is thermally stable.

As explained in Dr. Eliashevich's declaration, industry-standard thermal cycling and aging tests performed on the contact of Claim 1 demonstrated its thermal stability and lack of degradation. A00385. It demonstrated "remarkable" durability after thermal cycling. A00385.

3. The contact bonds well.

Furthermore, "[t]he surface morphology of the annealed n-contact is excellent, and correspondingly, the adhesion of the wire bond to the contact is

excellent." A00134. As explained in Dr. Eliashevich's declaration, the performance of the contact was remarkable because it performed consistently over the life of an LED. A00386. As a result, the contact was considered to have excellent and more than satisfactory thermal stability for a commercial product. A00386. The '215 patent provided a significant contribution to the field because it was the first Al-based contact to GaN which successfully satisfied the three criteria researchers sought for an n-type GaN-based LED. A00352,

B. The '215 Patent Represented A Major Technological Breakthrough In The Field Of Light Emitting Diodes.

The contact of the '215 patent achieved unprecedented combination of low contact resistance, thermal stability and wire bonding for an Al-based contact to n-type GaN. A00352-53. It also generated unexpected benefits of using Al as a base layer, and achieved success where many others – including Nichia and Dr. Nakamura – had failed for many years. A00352-53. By allowing the use of Al as a base layer in a low-resistance ohmic contact, the invention of the '215 patent opened the door to Al's inherent reflective qualities, which increase the efficiency of light extraction in an LED. A00352-53.

The contact of the '215 patent has stood the test of time. More than a decade after its invention, it is still used and praised by Nichia, which proclaims itself to be a pioneer and industry leader of the GaN LED field. A00352-53. Nichia's 219

series products have used the contact of the claimed invention from at least 2011 to the present. A00352-53.

STATEMENT OF THE CASE

Nichia petitioned for *inter partes* review in September 2012. A00002. The Board granted review of only one issue raised by Nichia: whether claims 1-17 of the '215 patent are unpatentable under 35 U.S.C. § 103(a) over JP10-256645 ("Kidoguchi"), U.S. Patent 5,563,422 ("Nakamura"), U.S. Patent 6,242,761 ("Fujimoto"), JP H08-274372 ("Shibata"), and the Admitted Prior Art. (Dkt. 13 at 15.) Emcore responded to the petition in May 2013, denying Nichia's claims of obviousness and challenging its construction of three key terms from Claim 1—"annealing," "base layer," and "barrier layer." A00263. Emcore simultaneously moved to amend the patent, A00726, asking the Board to cancel claims 2-5, 7-9, 12, 16-17, and replace these cancelled claims with proposed new claims 18-27.

Prior to the filing of the petition, Emcore and Everlight Electronics Co., Ltd., the exclusive licensee of the '215 patent, filed an infringement suit against Nichia in the United States District Court for the Eastern District of Michigan. *Everlight Electronics Co. v. Nichia Corp.*, No. 4-12-cv-11758 (E.D. Mich. filed Mar. 19 2012). The district court in that case held a *Markman* hearing in August 2013 and subsequently rendered an order construing the '215 patent. *Everlight Electronics Co.*, No. 4-12-cv-11758, ECF. No. 129 (E.D. Mich. Aug. 21, 2013). Notably, the

court construed the terms "annealing," "base layer," and "barrier layer." For all three, the court credited Emcore's construction over that of Nichia:

- Annealing—"heating the n-type III-V semiconductor, with the stack placed upon it, sufficiently to form a contact with low resistance." *Id.* at 17-21.
- Base layer—"the first-deposited metal layer used to form a low-resistance, ohmic contact to the semiconductor." *Id.* at 23.
- Barrier layer—"a layer provided to prevent undesirable results (e.g., diffusion) between the top layer and the base layer." *Id.* 21-23.

Following the *Markman* hearing, the '215 patent was dismissed via joint stipulation of the parties. *Everlight Electronics Co.*, No. 4-12-cv-11758, ECF. No. 260 (E.D. Mich. Mar. 19, 2014).

The Board held oral argument in this matter, A00776, and rendered a final written decision in February 2014. A00001. The Board held that claims 1-17 were obvious over a combination of Kidoguchi, Nakamura, Fujimoto, Shibata, and the Admitted Prior Art, and thus unpatentable under 35 U.S.C. § 103(a).

Beginning first with claim construction, the Board defined "annealing," "base layer," and "barrier layer" as follows:

- Annealing—"heating the semiconductor structure sufficiently to cause a change in some property of the semiconductor structure." A00013.

- Base layer—" the first-deposited metal layer used to form a contact to the semiconductor." A00015.
- Barrier layer—"a layer provided in between two layers to prevent undesirable reactions between the two layers." A00016.

The Board proceeded to find that the prior art disclosed key components of the '215 patent: a Al/Ti/Pt/Au electrode on an n-type GaN semiconductor, A0022-25, Pt and Ti barrier layers, A0025-26, and an annealed electrode, A00026-33. It further struck down claims directed towards the thickness of each layer of the stack, A00033-37, and the optimal time and temperature for annealing, A00038-40. The Board provided no specific explanation of how it was obvious to combine these elements together, noting only that "the combination of Kidoguchi, Nakamura, Fujimoto, Shibata, and the Admitted Prior Art" rendered the '215 patent obvious. A00025, 00026, 00033.

SUMMARY OF ARGUMENT

I. The Board erred in construing the claim terms "annealing" and "base layer" to omit any limitation relating to low contact resistance. The patent's written description makes it overwhelmingly clear that the purpose of the inventive method is the creation, not just of semiconductor contacts, but of semiconductor contacts with low resistance properties. By failing to give any consideration to the inventors' description of their invention in the specification, the Board failed to

follow the command of both 27 C.F.R. §42.300(b) and numerous decisions of this Court that claims are to be construed "in light of the specification." Its failure to construe the claims in light of the specification results in a patent that fails to implement the invention. In addition, the Board's constructions ignore extensive evidence in the written description associating the "annealing" step with the creation of low-resistance contacts, and fail to consider Nichia's admission in the *Everlight* litigation that "base layer" is properly construed to include a low-resistance limitation.

II. The Board's claim-construction errors were prejudicial and require reversal and remand to the Board for further proceedings using the correct constructions. Once the necessity of the low-resistance limitation is acknowledged, the Board's analysis—which for the most part assumes the absence of any such limitation—provides no basis to support the obviousness judgment. Of the prior art references on which the Board relied, only three purport to teach the annealing of an aluminum base layer and a gold top layer to produce a low-resistance contact. One of those, Luther, was not properly before the Board and so cannot be used to support the judgment. Once Luther is excluded, substantial evidence does not support the Board's obviousness determination. One of the remaining references, Shibata, is openly called into doubt by the other reference, Fujimoto, which attempted and failed to replicate Shibata's results. In light of Fujimoto, a person of

ordinary skill would not rely on Shibata. As for Fujimoto itself, that reference teaches neither annealing of an aluminum based contact to achieve low contact resistance nor any causal relationship at all between annealing and the creation of a low-resistance contact—which is what the correct construction of "annealing" requires. Similarly, with respect to "base layer," the primary reference on which the Board's decision relies—Kidoguchi—is expressly directed to the creation of *high*-resistance contacts. It does not teach annealing an aluminum base layer to achieve low resistance, and indeed is not even a relevant reference for that purpose.

III. Finally, even under the Board's erroneous claim constructions, the judgment of obviousness cannot stand. *First*, even if the Board was correct to omit any low-resistance limitation from the disputed terms in independent claim 1, a similar limitation is recited separately in dependent claim 15. Thus, all the grounds for reversal as to claim 1 under the correct claim constructions apply equally to claim 15 under the Board's constructions. *Second*, more broadly, neither Nichia nor the Board offered any evidence of motivation to combine the many disparate references on which their analysis relied. As a matter of law, a finding of obviousness requires more than the mere identification in the prior art of the individual elements of the claimed invention. A patent consisting of a new combination of existing elements may only be found obvious if the adjudicator can articulate some reason to combine the known elements in the fashion claimed by

the patent. Here, the Board provided no explanation at all for why a person of ordinary skill in the art would have combined (for example) Kidoguchi, which is directed to the fabrication of high-resistance contacts for use in lasers, with Fujimoto, which is directed to the fabrication of low-resistance contacts for use in LEDs. In the absence of some "articulated reasoning" to support that combination, the obviousness ruling cannot stand.

STANDARD OF REVIEW

In general, claim construction by the Board is a question of law that this Court reviews *de novo*, without deference. *See, e.g.*, *Rambus, Inc. v. Rea*, 731 F.3d 1248, 1252 (Fed. Cir. 2012). *But see In re Suitco Surface, Inc.*, 603 F.3d 1255, 1259 (Fed. Cir. 2010) (stating that review of a Board construction is limited to a determination of whether that construction is "reasonable.").

Obviousness is a question of law based on predicate questions of fact. The scope and content of prior art references is a factual question. *See, e.g.*, *Honeywell Int'l, Inc. v. United States*, 609 F.3d 1292, 1297 (Fed. Cir. 2010). In appeals from an IPR proceeding, factual findings will be upheld if they are supported by substantial evidence. *In re Suitco Surface,* 603 F.3d at 1259.

ARGUMENT

I. The Board Erred In Construing "Annealing" And "Base Layer."

The Board's invalidity judgment is predicated on erroneous constructions of the claim terms "annealing" and "base layer." In applying the "broadest

reasonable interpretation" standard of 37 C.F.R. § 42.300(b), the Board was required to give each disputed claim term the "broadest reasonable interpretation" "*in light of the specification of the patent in which it appears*." *Id*. (emphasis added). Consistent with the regulation, this Court has repeatedly instructed that the "broadest reasonable construction" must always "be consistent with the specification," and that "claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art." *In Re Abbott Diabetes Care*, 696 F.3d 1142, 1149 (Fed. Cir. 2012) (internal quotation omitted).

Here, the Board's constructions of "annealing" and "base layer" systematically ignored the command to interpret claims "in light of the specification." The patent's written description overwhelmingly teaches that the purpose of the inventive method is to use an aluminum base layer and annealing to produce *low-resistance* contacts that also feature good wire bonding. By construing the disputed terms "annealing" and "base layer" in ways that would cover a method of producing *high*-resistance contacts, the Board created a patent that fails to implement the invention. Specifically, with respect to "annealing," the Board's construction ignored extensive intrinsic evidence associating the "annealing" step with the production of low-resistance contacts. And with respect to "base layer," the Board ignored not only the specification, but Nichia's own

admission (in the *Everlight* case) that "base layer" should be construed as limited to the production of low-resistance contacts.

A. The Board's Constructions Result In A Patent That Is Inconsistent With The Specification And Fails To Implement The Invention.

At least since *Phillips*, this Court has recognized that every claim must be construed in light of the specification, and must be construed so that it "implement[s] the invention." *On Demand Machine Corp. v. Ingram Industries*, 442 F.3d 1331, 1344 (Fed. Cir. 2006). It has also recognized the propriety—and indeed the necessity—of considering the purpose of the invention, or the problem to be solved, in determining the meaning of a claim. *See, e.g.*, *Praxair, Inc. v. ATMI, Inc.*, 543 F.3d 1306, 1324 (Fed. Cir. 2008) ("The claims of the patent must be read in light of the specification's consistent emphasis on this fundamental feature of the invention.").[2]

Here, the specification states clearly that the problem to be solved is the tendency of existing methods of forming ohmic, low-resistance contacts to impair the reliability of the contact's gold bonds, and that the purpose of the invention is to provide a contact and a contact-forming method that both "provide a low resistance ohmic contact" ***and*** "allow reliable bonding of gold leads." A00133. A

[2] *See also, e.g.*, *Honeywell Int'l, Inc. v. U.S.,* 609 F.3d 1292, 1299 (Fed. Cir. 2010) (construing disputed claim term so as to implement "the fundamental purpose of the invention" as described in the specification); *Technology Patents LLC v. T-Mobile (UK) Ltd*., 700 F.3d 482, 493-94 (Fed. Cir. 2012) (same).

claim construction that covers contacts that lack low resistance or reliable bonding pushes the claim outside the scope of the disclosed invention, and into the prior art. It would not "implement the invention," and so could not be correct. *On Demand Machine*, 442 F.3d at 1344.

But that is precisely what the Board did here. To reach its constructions of "annealing" and "base layer," the Board had to ignore the inventors' description of their invention in the specification, which repeatedly and unequivocally explains that achieving low contact resistance is the invention's fundamental purpose. Absent a low-resistance limitation, the patent's claims are so divorced from the invention as to be meaningless.

1. The written description unequivocally demonstrates that the invention is directed to the fabrication of low-resistance contacts with good wire bonding.

To begin, the patent's Abstract describes the invention's method of making contacts and explains that "the resulting contact" has two key features: it provides both "a low-resistance, ohmic contact to the semiconductor" and "excellent bonding to gold leads." A00130.[3] The Background of the Invention then describes the desirability of two features of semiconductor contacts: first, the use of titanium and aluminum contact layers to produce contacts exhibiting "ohmic"

[3] A patent abstract is "a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains." MPEP 608.01(b). As such, it necessarily describes the inventive aspect of the patent—that is, the "invention."

characteristics and low contact resistance; and second, the use of gold-wire bonding in producing such contacts. A00133. It then explains the problem to be solved: namely, that "[a] contact including only titanium and aluminum would be incompatible with gold wire bonding," because "where a gold layer is provided on a contact containing titanium and aluminum, the gold layer can change during annealing," and "these changes impair the reliability of the wire bonds." A00133. The inventors then suggest the motivation for their invention: "it would be desirable to provide a contact and contact-forming method for n-type GaN and other n-type III-V semiconductors which would provide a low-resistance ohmic contact *and* which would also allow reliable bonding of gold leads such as gold wires to the contact." A00133 (emphasis added). That is, the invention's fundamental purpose is to use known materials to produce contacts that, when annealed, feature both low resistance and good wire bonding.

The Summary of the Invention continues the patent's emphasis on low contact resistance, noting that although "the present invention is not limited by any theory of operation," "whatever the mechanism of operation, the resulting contact has low resistance and ohmic behavior." A00133. That is, however the invention is implemented, it will *always* result in a low-resistance contact. This is consistent with everything else in the disclosure, all of which points to the conclusion that

achieving low contact resistance (together with reliable gold-wire bonding) is the whole point of the invention.

The descriptions of preferred embodiments only confirm this. At no point does the patent disclose any embodiment that *lacks* low contact resistance. Indeed, the patent only mentions the possibility of high contact resistance once—and then only to explain that high contact resistance will result in reduced efficiency, and so is undesirable. A00133.

In short, the intrinsic evidence overwhelmingly supports the conclusion that "the invention" relates to a method of creating low-resistance contacts—and only low-resistance contacts—that also feature good wire bonding.

2. By ignoring the written description of the invention, the Board's constructions result in a patent that fails to implement the invention.

In construing the claims, the Board actively ignored the regulatory and judicial command to interpret claims "in light of the specification," choosing instead to adopt generic constructions of "annealing" and "base layer" that are wholly divorced from the disclosed invention.

On "annealing," the Board suggested that in the absence of an express act of lexicography giving a term a meaning "that is different from its recognized meaning to one of ordinary skill in the art," claim terms should be construed generically, without reference to the patent's disclosure: "The claim language used

by Emcore is broad. One with ordinary skill in the art may use 'annealing' to form a contact that does *not* have low resistance contact [sic] or to form other semiconductor structures." A00010-11 (emphasis added). Consistent with that view, the Board construed "annealing" without reference to any feature of the invention, to mean "heating the semiconductor structure sufficiently to cause a change in some property of the semiconductor structure." A00013. That construction would cover an annealing step that results in an increase in contact resistance, or a degradation in the gold wire layer—two consequences that the invention expressly aims to avoid.

Under the Board's approach, absent an express definition in the specification, "annealing" should be construed to have the exact same meaning they would have if the patent did not exist. This is simply not consistent with the regulatory command to give claims the "broadest reasonable interpretation *in light of the specification*." 37 C.F.R. §42.300(b); *see, e.g.*, *Tempo Lighting, Inc. v. Tivoli LLC*, 742 F.3d 973, 978 (Fed. Cir. 2013). Where, as here, the express purpose of the disclosed invention is to achieve a particular result, a claim construction that covers the opposite result fails to "implement the invention," and cannot be correct. *On Demand Machine*, 442 F.3d at 1344.

The Board made the same error with "base layer." There, in response to Emcore's proposal that the term be limited to base layers used in forming low-

resistance contacts, the Board reiterated its evident belief that the inventors' description of the invention has no role in construing the claims. The Board pointed to the Background section of the patent—the part that does *not* describe the invention—which explains that as a general matter, "in *most* semiconductor devices, . . . the contact *desirably* has low resistance." A00014 (emphasis added). Relying on that language, the Board concluded that "the goal of forming a low-resistance, ohmic contact is desirable, but not all semiconductor devices have such desirable characteristics," and on that basis declined to limit the claimed base layer to the low-resistance context. A00015. In other words, the Board concluded that because not all semiconductor devices use low-resistance contacts, the devices used *in the invention* need not use them either. Accordingly, the Board construed "base layer" independently of the invention in which it appears, to mean "the first-deposited metal layer used to form a contact to the semiconductor." A00015.

This is almost a parody of claim construction: the Board intentionally construed the disputed terms so as to divorce them from the invention. Again, this approach cannot be reconciled with the requirements of § 42.300(b) or this Court's repeated instructions to interpret claims consistent with the specification, so as to implement the invention.

B. Both "Annealing" And "Base Layer" Are Properly Limited To The Creation Of Low-Resistance Contacts.

The evidence is overwhelming that the invention *as a whole* is directed to the production of low-resistance contacts with good wire bonding. As explained above, sound claim-construction principles require that the claims be interpreted consistent with that purpose. Lest there be any doubt about that conclusion, however, we now demonstrate that the *individual terms* "annealing" and "base layer" are themselves properly construed as limited to the fabrication of low-resistance contacts.

1. The written description specifically associates "annealing" with the creation of "low resistance" contacts.

Consistent with its emphatic emphasis on the creation of low-resistance contacts, the patent's "specification makes clear that the annealing step produces the beneficial change of forming a low resistance contact." *Everlight Electronics Co.*, No. 4-12-cv-11758, ECF. No. 129, at 20 (E.D. Mich. Aug. 21, 2013).

For example, the written description states that "after deposition, layers 34-40 constituting the in-process contact or stack are annealed. Annealing is required from a low-resistance contact." A00134. It then explains that "moderate temperatures of 400-600 C are sufficient for low contact resistances of the order of 10^{-5} ohm-cm^2 or lower." A00134. There are no disclosed examples of annealing

resulting in anything other than a low-resistance contact—which is precisely what one would expect, given the centrality of low resistance to the invention itself.[4]

Faced with this overwhelming specification evidence associating the "annealing" step with low contact resistance, the *Everlight* court adopted the construction advocated here by Emcore: "heating the n-type III-V semiconductor, with the stack placed upon it, sufficiently to form a contact with low resistance." *Everlight Electronics Co.*, No. 4-12-cv-11758, ECF. No. 129, at 18, 21. The Board had the benefit of the District Court's Markman Order, but never mentions it in reaching the opposite result. The Board's contrary construction is erroneous: The patent's disclosure simply leaves no room for a construction of "annealing" that would cover a process in which annealing did not result in low contact resistance.

The Board's construction of "annealing" is also wrong for a second, independent reason. By construing "annealing" to mean "heating the semiconductor structure sufficiently to cause a change in some property of the semiconductor structure," the Board would permit claim 1 to cover an annealing operation that causes the gold layer to change *in any way*—including ways that are wholly undesirable from the perspective of fabricating LEDs. Indeed, the Board's construction would cover annealing that "impairs the reliability of the wired

[4] In addition, the Lin reference, which is specifically referred to in the written description, also describes "a new metallization process for achieving low resistance ohmic contacts," in which annealing plays a significant role in achieving low contact resistance.

bonds"—which is exactly the problem the patent purports to solve. A00133. A construction that would result in the occurrence of the very problem the invention exists to solve is necessarily incorrect.

In rejecting Emcore's proposed construction, the Board relied in part on claim differentiation, observing that claim 15 claims "a contact resistance of less than about 10^{-5} ohm-cm^2" and that including a low-resistance limitation in "annealing" and "base layer" would render claim 15 "insignificant, if not wholly superfluous." A00012. That conclusion was incorrect.

Assuming, for the sake of argument, that a claim construction requiring "low resistance" renders superfluous a dependent claim reciting a *particular* low resistance, that fact would not end the inquiry. Rather, the doctrine of claim differentiation merely raises a *presumption* that the limitation in the narrower claim should not be read into the broader one. *Retractable Techs., Inc. v. Becton, Dickinson and Co.*, 653 F.3d 1296, 1305 (Fed. Cir. 2011). That presumption, moreover, is a weak one: as this Court has explained, "any presumption created by the doctrine of claim differentiation will be overcome by a contrary construction dictated by the written description or prosecution history." *Id.*

Here, as we have shown, the written description overwhelmingly dictates the conclusion that the claimed method applies only to the creation of low-resistance

contacts. The specification's exclusive emphasis on the low-resistance feature easily overcomes any claim differentiation presumption created by Claim 15.

2. Nichia conceded in the *Everlight* litigation that "base layer" should be construed to include a low-resistance limitation.

The same analysis holds for the construction of "base layer." Given the invention's purpose, it would be strange if the claimed "base layer" could be construed to cover anything but layers that are conducive to low resistance. And elsewhere, Nichia has *agreed* that "base layer" should include a low-resistance limitation. In *Everlight*, Nichia proposed that "base layer" be construed to mean "the first-deposited metal layer used to form a *low-resistance, ohmic* contact to the semiconductor, and being in direct contact with a top surface of the n-type III-V semiconductor." *Everlight Electronics Co.*, No. 4-12-cv-11758, ECF. No. 111, at 22; *Everlight Electronics Co.*, No. 4-12-cv-11758, ECF. No. 129, at 23. The first clause of that proposed construction is identical to the construction Emcore advocates here.

Now, however, Nichia argues neither the "ohmic" nor the "low resistance" limitations were properly included in the construction of "base layer": in the hearing, Nichia's counsel said that "there's no basis to introduce ohmic into claim 1," and that "low resistance presents some challenges for Emcore," because "as

soon as you introduce that concept into claim 1, you've got a claim differentiation problem" with claim 15.[5] A00786.

Neither the claims nor the written description changed between July 2013, when Nichia argued *for* the inclusion of "ohmic" and "low resistance" limitations in the District Court, and November 2013, when Nichia argued (successfully) *against* the inclusion of those exact limitations before the Board. Even if Nichia was not judicially estopped from completely reversing its position in the second proceeding, its proposed construction in District Court operates as an admission that the construction of "base layer" properly includes the "ohmic, low resistance" limitation that the Board, at Nichia's urging, declined to adopt.

II. The Board's Claim Construction Errors Were Prejudicial And Require Reversal Of The Invalidity Judgment And Remand.

In most circumstances, "a change in the claim construction by the Federal Circuit" will "require a remand to the district court to rule on the infringement or invalidity question under the proper claim construction," for the simple reason that parties typically do not dispute claim constructions unless the differences in their proposed constructions are consequential. 6 Ann. Pat. Digest § 40.65 (2014). That general principle holds true here. If "annealing" and "base layer" are properly construed to include the low resistance limitation that the written description

[5] As explained Section I.B(1), *supra*, the clarity of the specification's commitment to the creation of low-resistance contacts overcomes any presumption that might arise from the doctrine of claim differentiation.

overwhelmingly supports, then the evidence proffered by Nichia below is inadequate to prove that the '215 patent, "as a whole[,] would have been obvious at the time the invention was made to a person having ordinary skill in the art." *In re Glatt Air Techniques, Inc.*, 630 F.3d 1026, 1029 (Fed. Cir. 2011).

This is true for two reasons. *First*, one of the primary references that the Board claimed taught the use of annealing an aluminum base layer to form a low-resistance contact—the Luther reference—was not properly before the Board. As a matter of law, that reference cannot be used to support an obviousness rejection. *Second*, once Luther is excluded, the remaining prior art simply is not sufficient to support the rejection.

A. Because The Luther Reference Was Not Properly Before The Board, It Cannot Be Used To Support The Obviousness Rejection.

The Board may only enter a final written decision upon "any patent claim challenged by the petitioner and any new claim added under section 316(d) [*i.e.*, a motion to amend the patent." 35 U.S.C. § 318(a). To challenge a patent claim properly, the petitioner ***must*** comply with the strictures of 35 U.S.C. § 312. *Id.* § 312 ("A petition filed under section 311 may be considered [by the Board] *only if* . . . ." (emphasis added)). Under that rubric, the petitioner must "identif[y], in writing and with particularity, each claim challenged, the grounds on which the challenge to each claim is based, *and the evidence that supports the grounds for the challenge to each claim*." 35 U.S.C. § 312(a)(3) (emphasis added). The

petitioner must also include "copies of patents and printed publications that the petitioner relies upon in support of the petition." *Id.* § 312(a)(3)(A). While the petitioner may submit supplemental information in accordance with 35 U.S.C. § 316(a)(3), that evidence may only be submitted upon filing a "request for the authorization to file a motion to submit supplemental information." 37 C.F.R. § 42.123(a).

Here, Nichia did not submit Luther, A00762, to the Board as part of its petition for inter partes review. Nor did Nichia seek permission to supplement the record via 37 C.F.R. § 42.123(a). Instead—and as Nichia admits—Luther was not submitted to the Board until Nichia filed its opposition to Emcore's motion to amend. A00842-43. Accordingly, by the black letter of the law, the Luther reference was not properly before the Board. Indeed, at oral argument, the Board acknowledged that §312 required Nichia to make its invalidity case using only the evidence in its initial petition:

> Mr. Tomasulo: And it's our understanding that Nichia was required to make its case *in its petition*, to carry the burden *in its petition*. Is that correct?
>
> Judge Chang: Yes.

A00815 (emphasis added).

That, however, did not stop the Board from using Luther as one of the primary references over which it invalidated the claims. For example, Luther is

cited prominently in the Board's obviousness analysis on "annealing," which states that "Luther reported on a study of Al and Ti/Al contacts to n-type GaN that achieved a low contact resistivity of 8 x 10^{-6} Ωcm^2 and good thermal stability." A0031-32. Perhaps more important, the Board pointed to Luther as the main evidence leading it to discredit Emcore's expert testimony and bolster the dubious reliability of its single most important prior art reference, Shibata:

> Given that Shibata and Luther show that others have achieved low contact resistance and good thermal stability by annealing Al contacts to n-type GaN, the testimony of Emcore's expert—that one of ordinary skill in the art would not have understood Shibata as teaching a low resistance ohmic contact to n-type GaN [A00349]—is entitled little weight.

A00032. That was error. While the Board may well be able to assess more weight to a prior publication than an expert's subsequent testimony, *see* A00032 (citing *Velander v. Garner*, 348 F.3d 1359, 1371 (Fed. Cir. 2003)), it may not do so based upon evidence not properly before it.

B. Once Luther Is Excluded, Substantial Evidence Does Not Support The Board's Obviousness Determination With Respect To "Annealing."

Without Luther, the Board's finding of the obviousness of annealing a gold-topped, aluminum-based stack to achieve low contact resistance falls apart.[6]

[6] As discussed below, the Board's reasoning is dubious even *with* Luther, as that reference (like many others) address aluminum-based stacks *without* gold tops. The degradation of the gold top during the annealing process is the key problem that the '215 patent solves.

Indeed, much of it fell apart long before the Final Written Decision issued. The Board's decision instituting review cited the Nakamura reference for its conclusion that "annealing Al-Au based contacts was well known in the art at the time of the invention." A00256. But as Nichia's expert later acknowledged, Nakamura teaches no such thing: the relevant passage of Nakamura discusses the annealing of the semiconductor itself, not a semiconductor contact, and so has nothing to do with the contact annealing at issue here. A00541-42. The decision instituting review was thus based in large part on a fundamental misunderstanding of the prior art.

By the time of the final decision, the Board's analysis of the annealing step relied on only two references: Shibata and Fujimoto. Neither of those references in fact teaches annealing a contact featuring both an Al base layer and an Au top layer to achieve low resistance.

1. A person of ordinary skill would not rely on Shibata in light of Fujimoto's inability to replicate Shibata's results.

The Board relied heavily on the Shibata reference, an unexamined Japanese patent application, finding that Shibata taught both that "annealing an Al/Ti/Au electrode on an n-type GaN semiconductor under certain conditions would achieve low contact resistance and good ohmic contact," and that "using a barrier layer that has an optimal thickness would prevent the purported 'annealing' problem." A00032. In effect, the Board found that Shibata taught both the full scope of claim

1 (including the base layer, barrier layers, gold layer, and annealing steps) and the critical aspects of the invention that are not expressly claimed there—low contact resistance, good ohmic contact, and good wire bonding.

That finding, however, is greatly undermined by Nichia's own evidence, in the form of the other reference on which the Board primarily relied—Fujimoto. Following the publication of Shibata in 1995, Fujimoto—working for semiconductor giant Toshiba—attempted to replicate Shibata's experiments. He was unable to do so. As the Fujimoto reference explains:

> There are various proposals on the electrode to the n-type layers. For example, Japanese Patent Laid-Open Publication No. 3-252175 discloses aluminum (Al). **The use of aluminum, however, invites decomposition or deterioration during various annealing steps after deposition of the electrode, and degrades wire bonding**. Japanese Patent Laid-Open Publication No. 7-240508 teaches stacking gold (Au) on an Al electrode to facilitate wire bonding. However, **the Inventors have experimentally recognized that deterioration or decomposition still remains unsolved because Au and Al are mixed or oxidized during annealing.**

A000185 (emphasis added).

Fujimoto's conclusions are notable because they are in line with all the other prior art in the field. Other than the inadmissible Luther, neither Nichia nor the Board has ever pointed to any teaching in the remaining prior art that suggests annealing an aluminum-based stack, let alone an Al/Au stack, in a manner that does not suffer from poor wire bonding or unacceptably high contact resistance.

To the contrary, all the prior art squarely teaches *away* from the '215 patent's invention.

For example, Nakamura notes that, "[I]t has been found that aluminum and indium can hardly establish an ohmic contact with the n-type gallium nitride based III-V Group compound semiconductor layer, and tend to degrade by an annealing treatment, losing the electrical conductivity." A00208. The troubles experienced by Nakamura comport with the Admitted Prior Art in Emcore's provisional patent application, which states that annealing contacts with an aluminum base layer is "accompanied by degradation in the surface morphology, due to metallurgical reactions between the metal layers in the stack" and can lead to "device failure." A00172. And, indeed, Nichia's own expert admits that the prior art serves as a "warning" that annealing an Al-based contact could lead to "device failure." A00701-02.

The significance of this is quite simple: a person of ordinary skill in the art would look upon the clear teachings away from annealing announced by the prior art, and would look to Fujimoto's clear warning regarding the reliability of Shibata, and would conclude that annealing is not a desirable, let alone required, step in creating a n-GaN LED—the exact opposite of what the '215 patent demonstrates. A00135.

The Board dismissed Fujimoto's criticism of Shibata, faulting Emcore for not "provid[ing] any experimental data regarding the alleged experiment conducted by Fujimoto." A00031. But that gets the applicable burden of proof precisely backwards. It is not Emcore's obligation to explain why a manifest conflict in Nichia's *own evidence* should break in Emcore's favor. Rather, "[i]n an inter partes review . . . , the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence." 35 U.S.C. § 316(e). To the extent that Fujimoto casts doubt upon Shibata—the only piece of competent evidence in the record that gives Nichia a colorable prior-art claim on annealing—it was Nichia's responsibility to explain Fujimoto away.[7] The Board's decision to shift that burden to Emcore is plain and reversible error. *See Rambus Inc. v. Rea*, 731 F.3d 1248, 1255 (Fed. Cir. 2013) (holding the Board committed reversible legal error by "placing the burden on [the patent owner] that its claims were not obvious").[8]

[7] And to the extent that Fujimoto suffered from any deficiencies, Shibata suffered from greater deficiencies, e.g., lack of experimental results and a measurement that purported to be "contact resistance" but could not be given the unit of measurement.

[8] As discussed above, the Board also attempted to shore up its reliance on Shibata by pointing to similar disclosures in Luther—using an inadmissible reference to bolster an unreliable one. A00031-32.

2. Fujimoto does not teach "annealing" of an Al/Au contact to effect low resistance.

The Board's last line of defense—both in its defense of Shibata and its obviousness analysis—is Fujimoto, which the Board found "teaches annealing a multi-layered electrode—that includes an Al base layer—at a certain temperature range, to form a nitride compound semiconductor light emitting device having a *low contact resistance and good wire bonding*." A00029 (emphasis original). But that description is inaccurate for two reasons.

First, the inventors of Fujimoto did *not* achieve low contact resistance with an aluminum based contact. The Fujimoto disclosure indicates that in annealing an Al/Au stack, the resulting product had a contact resistance of $10^{-4}\Omega cm^2$. A00192. The parties' experts agreed that the threshold for "low" contact resistance is $10^{-5}\Omega cm^2$, (A00157 (Schubert); A00382(Goorsky)), meaning that the disclosed resistance achieved in Fujimoto is an order of magnitude worse than the agreed standard for low resistance. Indeed, for one skilled in the art who seeks low contact resistance, Fujimoto teaches *away* from aluminum and towards either copper or silver. A00194.

Second, Fujimoto does not teach a causal relationship between annealing and low contact resistance. Rather, it simply notes that annealing is "prefer[ed]" A00192. Under a proper construction of "annealing," that is not enough. The '215 patent requires not merely that the fabrication method *include* both annealing and

low resistance. Rather, it requires that the heating be "*sufficient[ ] to form* a contact with low resistance." That is, the correct construction requires that there be a *causal relationship* between annealing and low resistance. Fujimoto does not teach such a causal relationship: there is simply nothing in Fujimoto to suggest that annealing itself creates a low-resistance contact.

C. Substantial Evidence Does Not Support The Board's Obviousness Finding With Respect To "Base Layer."

The absence of any valid prior art teaching the "annealing" step is sufficient to require reversal of the obviousness judgment. The same deficiency, however, also applies under a correct construction of "base layer," thus providing a second and independent ground for reversal.

The primary reference cited by the Board supporting the obviousness of the "base layer" element was Kidoguchi. A00022-25. Although Kidoguchi primarily describes using Mo as the base layer, it includes a single, conclusory sentence indicating that various "other metals such as W, Ta, Ti, or Al, for example, may also be used." A00226-27. Based on this single sentence, the Board concluded that Kidoguchi fully taught the use of an aluminum base layer as claimed in the '215 patent. A00022-23.

Even if that conclusion were correct under the Board's construction of "base layer," it is plainly wrong under the correct construction. There is no question that Kidoguchi does not teach the use of an aluminum base layer to create a *low-*

resistance contact, as the correct construction requires. To the contrary, Kidoguchi is expressly directed to the fabrication of *high*-resistance contacts.[9] *See, e.g.*, A00226-28.

The only other references cited by the Board with respect to "base layer"—in conclusory fashion—were Shibata, the Admitted Prior Art, and Fujimoto. We have already addressed the deficiencies of Shibata and Fujimoto. As to the Admitted Prior Art, while it does describe the use of aluminum as a base layer in low-resistance contacts—it specifically teaches that its use causes the very problem the claimed invention solves: the deterioration of wire bonds and device failure. A00172; *see* A00130 (describing the invention as a method of producing both "a low-resistance, ohmic contact" and "excellent bonding to gold leads"). Fujimoto states the same, explaining that the use of an aluminum base layer "invites decomposition or deterioration during various annealing steps." A00185. And as noted above, the contact resistance achieved by Fujimoto falls well short of what all parties agree is the threshold for "low" contact resistance. A00157 (Schubert); A00382(Goorsky).

In other words, a person of ordinary skill in the art reading the Admitted Prior Art and Fujimoto would understand that he or she could use an aluminum

[9] Indeed, once the importance of low resistance is acknowledged, Kidoguchi—focused as it is on the creation of high-resistance contacts for use in lasers—is not even an appropriate prior art reference for the '215 patent.

base layer—but would also understand that doing so would prevent the creation of reliable wire bonds. Thus, the prior art did teach the use of aluminum as a base layer, but it also taught that a person of ordinary skill seeking to achieve the claimed invention *would never have used it*. The Board's obviousness judgment on "base layer" is thus a product of impermissible hindsight bias.

III. Even Under The Board's Claim Constructions, The Judgment Cannot Stand.

Regardless of whether Luther was properly admitted (and especially if it was not), the Board's decision still does not pass muster, for at least two reasons. First, even if "annealing" and "base layer" are construed without any low-resistance limitation—thus omitting that limitation from independent claim 1—dependent claim 15 separately claims low resistance, so all of the reasons set forth above in Section II demonstrating why the asserted prior art references do not teach low resistance apply equally to claim 15. Second, while the Board allegedly locates the various elements comprising the '215 patent in the prior art, neither the Board nor Nichia highlight any evidence of a motive to combine these elements. This is particularly significant here, where the prior art reveals a clear tension between the Al/Au stack (necessary for quality wiring) and the annealing process (necessary for lowered resistance).

A. All The Reasons For Reversal Under The Correct Claim Constructions Apply Equally To Dependent Claim 15 Under The Board's Claim Construction.

Even if "annealing" and "base layer" are not construed to require low resistance, the low-resistance limitation remains present in the patent in the form of claim 15. That claim recites "A method as claimed in claim 1 wherein said Al/Ti/Pt/Au contact has a contact resistance of 10^{-5} ohm-cm^2." A00135. As noted, both parties' experts agree that 10^{-5} ohm-cm^2 constitutes "low" contact resistance. A00010-11.

In finding claim 15 obvious, the Board relied primarily on Shibata. A00011. We have already explained that Shibata is not a reliable reference: when it is considered in light of Fujimoto's failure to replicate its results (and its inconsistency with all the art coming before it), a person of ordinary skill would not rely on its disclosure as teaching the achievement of low resistance. *See* Section II.B.1, *supra*. Claim 15 is non-obvious under the Board's erroneous claim constructions for the same reasons claim 1 is non-obvious under the correct claim constructions.

B. The Board Failed To Articulate Any Reasoned Motivation To Combine The Various References.

As this Court has rightly noted, "[m]ost if not all inventions arise from a combination of old elements" and thus "every element of a claimed invention may often be found in the prior art." *In re Kotzab*, 217 F.3d 1365, 1369-70 (Fed. Cir.

2000). However, "identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention." *Id.* at 1370. Rather, a patent comprising of a new combination of prior art will only be found obvious if prior art reveals "an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *Ecolab, Inc. v. FMC Corp.*, 569 F.3d 1335, 1350 (Fed. Cir. 2009), *amended in non-pertinent part*, 366 F. App'x 154 (Fed. Cir. 2009) (citing *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007)).

The Board never explains how one of ordinary skill in the art would be motivated to combine the various references cited in the Board's obviousness finding.[10] That alone is error: "[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *InTouch Techs., Inc. v. VGO Commc'ns, Inc.*, 751 F.3d 1327, 1347 (Fed. Cir. 2014) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). While,

[10] As noted, supra, the supposed rationale for combining these references articulated in Nichia's Petition – and adopted by the Board's decision instituting review – was abandoned by both Nichia and the Board. Specifically, both Nichia and the Board originally relied on the Nakamura reference to support the conclusion that "annealing Al-Au based contacts was well known in the art at the time of the invention." A00256. But as Nichia's expert later acknowledged, Nakamura teaches no such thing: the relevant passage of Nakamura discusses the annealing of the semiconductor itself, not a semiconductor contact, and so has nothing to do with the contact annealing at issue here. A00541-42. Once the erroneous reliance on Nakamura was abandoned, neither Nichia nor the Board could find any motivation at all to combine the references.

to be sure, an "obviousness determination is not the result of a rigid formula disassociated from the consideration of the facts of a case," *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1161 (Fed. Cir. 2007), the Board most articulate some rationale for finding the combination of the prior art obvious. "The requirement of such an explanation is consistent with governing obviousness law and helps ensure predictable patentability determinations." *In re Kahn*, 441 F.3d at 987 (citations omitted). Moreover, it ensures that the Board has not fallen prey to "the distortion caused by hindsight bias." *KSR Int'l Co.*, 550 U.S. at 421.

Here, even if we assume *arguendo* that the prior art reveals every element of the '215 patent, the Board's opinion provides no explanation of why it would be obvious to combine those pieces together in the fashion presented in the '215 patent. Instead, the Board simply *asserts*—repeatedly—that "the combination of Kidoguchi, Nakamura, Fujimoto, Shibata, and the Admitted Prior Art would have rendered obvious to one with ordinary skill in the art the claimed invention." A00025, 00026, 00033.. Repeating the same phrase three times does not transform a conclusory statement into the "articulated reasoning" required under *InTouch Techs., Inc.*, 751 F.3d at 1347.

Because the Board failed to offer any semblance of meaningful analysis, we are simply left to guess why it found the motive to combine the prior art to be obvious. Under *InTouch Techs.*, that is not enough to support a judgment of

obviousness. In any event, even if the Board had attempted to identify a motivation to combine, it could not have done so. Nichia, who bore the burden of providing such a motivation, made no attempt to provide one, and for good reason. Kidoguchi, for example, is directed to high-resistance contacts for use in lasers, focuses primarily on using a base layer of molybdenum, and recites the use of aluminum base layer only in passing, without explanation. A00226-27. No one, and certainly not the Board, has offered a credible explanation for why a person of ordinary skill in the art looking to solve the problems caused when annealing an aluminum base layer to produce a low-resistance contact in an LED would look to Kidoguchi or think to combine it with wholly different LED-related art.

Nor does the record support a finding of motivation to combine Shibata with the other references—especially Fujimoto. Nichia relied on the combination of Shibata and Fujimoto to teach the steps of dependent claims 6-10 and 16-17. A00033. But neither Nichia or the Board ever explained why a person of ordinary skill in the art, knowing that Fujimoto has called into question the accuracy of Shibata's disclosures, would think to combine those references for any reason.

The absence of any findings articulating a valid motion to combine the various prior art references is fatal to the judgment of obviousness. That judgment must be reversed.

CONCLUSION

For all the reasons given, Emcore respectfully requests that the judgment of the Board be REVERSED and the case REMANDED to the Board for further proceedings.

Dated: August 27, 2014

Respectfully Submitted,

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ADDENDUM

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571-272-7822

Paper 68
Entered: February 11, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NICHIA CORPORATION
Petitioner

v.

EMCORE CORPORATION
Patent Owner

Case IPR2012-00005
Patent 6,653,215

Before KEVIN F. TURNER, STEPHEN C. SIU, and JONI Y. CHANG, *Administrative Patent Judges*.

CHANG, *Administrative Patent Judge*

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

Nichia Corporation ("Nichia") filed a petition on September 16, 2012, requesting an *inter partes* review of claims 1-17 of U.S. Patent No. 6,653,215 ("the '215 patent"). Paper 2 ("Pet."). The patent owner, Emcore Corporation ("Emcore") did not file a preliminary response. Upon review of Nichia's petition, the Board instituted this trial on February 12, 2013.

During the trial, Emcore filed a patent owner response (Paper 24 ("PO Resp.")), and Nichia filed a reply to the patent owner response (Paper 38 ("Pet. Reply")). Emcore also filed a motion to amend claims (Paper 26); Nichia filed an opposition to Emcore's motion to amend claims (Paper 40); and Emcore then filed a reply (Paper 43) to Nichia's opposition. Oral hearing was held on November 6, 2013.[1]

We have jurisdiction under 35 U.S.C. § 6(c). This final written decision is entered pursuant to 35 U.S.C. § 318(a). We hold that claims 1-17 of the '215 patent are unpatentable under 35 U.S.C. § 103(a). Emcore's motion to amend claims is denied.

A. Related Proceeding

Nichia indicates that the '215 patent is asserted in the litigation styled *Emcore Corp. v. Nichia Corp.*, Case No. 2-12-cv-11758 (E.D. Mich). Pet. 1.

[1] A transcript of the oral hearing is included in the record as Paper 66.

B. Real Party-in-Interest

Emcore asserts that Nichia[2] failed to identify all real parties-in-interest in the petition, as required by 35 U.S.C. § 312(a)(2). PO Resp. 1. In support of that assertion, Emcore alleges that Nichia represented to the district court, in a motion to stay, that both Nichia Corporation and Nichia America Corporation ("NAC") filed the petition. *Id*. at 2 (citing Ex. 2017, 1). Emcore takes the position that the petition was "filed at the behest of both Nichia Corporation and NAC," and that Nichia "is acting in the interest of NAC." *Id*. at 3. Emcore submits that NAC is a subsidiary of Nichia, and as co-defendants in the district court litigation, both Nichia and NAC used the same expert witness and counsel, and asserted the same prior art and claim for a declaratory judgment. *Id*. at 3-4.

Nichia disagrees and argues that a clerical error was made inadvertently in the motion to stay, and it has notified the district court of the clerical error. Pet. Reply 15. As support, Nichia has submitted a copy of the Notice Correcting Corporate Names (Ex. 1036) that was filed in the district court. *Id*. Nichia also asserts that NAC had no control over the decision to file a petition, drafting the petition, or the content of the petition. *Id*. at 14. Nichia further maintains that NAC did not fund the petition. *Id*.

We are not persuaded by Emcore's argument, as it is based on a clerical error made in a Nichia's court filing, and speculations. Whether a party that is not named in an *inter partes* review is a "real party-in-interest"

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[2] In the instant proceeding, the term "Nichia" refers to Nichia Corporation, and does not include Nichia America Corporation.

is a "highly fact-dependent question," taking into account various factors such as whether the non-party "exercised or could have exercised control over a party's participation in a proceeding" and the degree to which a non-party funds directs and controls the proceeding. Office Patent Trial Practice Guide, 77 Fed. Reg. 48756, 48759-60 (Aug. 14, 2012).

Upon review of the parties' arguments and evidence, we determine that Emcore did not demonstrate adequately that Nichia failed to identify all real parties-in-interest. The petition identifies Nichia Corporation as the real party-in-interest. Pet. 1. Nichia's motion to stay (Ex. 2017) and the Notice Correcting Corporate Names (Ex. 1036) reveal that: (1) the motion to stay used the shorthand "Nichia" to refer to both Nichia Corporation and NAC; (2) the motion to stay inadvertently stated that "Nichia filed a Petition for *inter partes* review . . ."; and (3) the motion to stay should have used "Nichia Corporation" rather than "Nichia." Ex. 2017, 1-2; Ex. 1036, 2. The evidence before us clearly shows that the motion to stay filed in the district court contains a clerical error, especially in light of the fact that in the instant proceeding, we use the term "Nichia" to refer only to Nichia Corporation (*see, e.g.*, Decision on Institution, Paper 13 at 2). Therefore, the evidence does not establish that NAC is a real party-in-interest to this proceeding. Moreover, the mere fact that Nichia and NAC, as co-defendants, shared the same counsel and expert witness, and had similar litigation strategy is not sufficient to prove that NAC exercised, or could have exercised, control over Nichia's action in the instant proceeding. Nor does being a subsidiary of Nichia establish that NAC has the ability to control Nichia's conduct in this

proceeding, in the absence of any evidence of contractual obligations of the parties. For the foregoing reasons, Emcore fails to demonstrate that Nichia did not identify all real parties-in-interest in the petition.

C. The '215 Patent

The '215 patent is directed to a method of forming a contact on an n-type III-V semiconductor by depositing four layers of metal and annealing the resulting stack. Ex. 1001, Abs. Figure 3 is a sectional view of a contact, and is reproduced below (with labels added, *see* Ex. 1001, 4:32-36):

FIG. 3

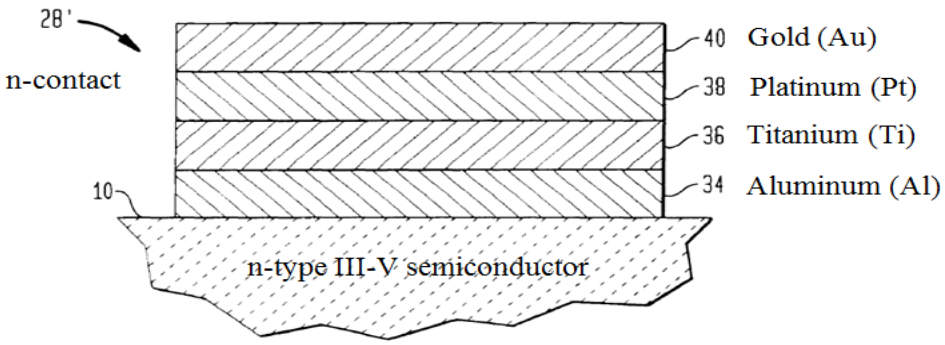

Figure 3 shows a contact formed in accordance with the claimed method.

Claim 1, reproduced below, is the sole independent claim:

> A method of forming a contact on an n-type III-V semiconductor comprising the steps of:
>
> (a) depositing Al on the n-type III-V semiconductor to provide a base layer; then
>
> (b) depositing Ti on said base layer to provide a first barrier layer; then
>
> (c) depositing Pt on said first barrier layer to provide a second barrier layer; then
>
> (d) depositing Au on said second barrier layer to provide

a top layer, whereby said base layer, said first barrier layer, said second barrier layer, and said top layer form a stack on the n-type semiconductor; and then

(e) annealing said n-type III-V semiconductor with said stack thereon.

D. Prior Art Relied Upon

Nichia relies upon the following prior art references:

Fujimoto	U.S. 6,242,761	Jun. 5, 2001	(Ex. 1007)
Nakamura	U.S. 5,563,422	Oct. 8, 1996	(Ex. 1013)
Kawamura	JP H06-37036	Feb. 10, 1994	(Ex. 1014 & 1015)
Kidoguchi	JP10-256645	Sept. 25, 1998	(Ex. 1016 & 1017)[3]
Shibata	JP H08-274372	Oct. 18, 1996	(Ex. 1018 & 1019)[4]

Admitted Prior Art – the background section of '215 patent (Ex. 1001, 1:15-2:9) and the background section of provisional application 60/238,221 ("the '221 provisional application") (Ex. 1004, 1-2[5]).

Murarka, et al., "Investigation of the Ti-Pt Diffusion Barrier for Gold Beam Leads on Aluminum," 125 Iss.1 J. Electrochem. Soc. 1561978 (Ex.1008).

Vendenberg, et al., "An in situ x-ray study of gold/barrier-metal interactions with InGaAsP/InP layers,"55(10) J. Appl, Phys. 3676 (15 May 1984) (Ex.1009).

Lepselter, "Beam-Lead Technology," 45, The Bell System Technical Journal 233 (1966) (Ex.1020).

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[3] The exhibits provide the specified Japanese patent application and a certified English translation thereof, where we cite to the English translation.

[4] *Ibid.*

[5] All references to the page numbers of the '221 provisional application refer to the original page numbers, and not the exhibit page numbers.

Terry, et al., "Metallization Systems for Silicon Integrated Circuits," 57, No. 9 Proc. IEEE 1580 (1969) (Ex. 1021).

Hoff, et al., "Ohmic contacts to semiconducting diamond using a Ti/Pt/Au trilayer metallization scheme," 5 (1996) Diamond and Related Materials 1450 (Ex. 1022).

Durbha, et al., "Thermal Stability of Ohmic Contacts to n-$In_xGa_{1-x}N$," 395 Mat. Res. Soc. Symp. Proc. 825(1996) (Ex. 1023).

E. Ground of Unpatentability

The Board instituted the instant trial based on the ground that claims 1-17 of the '215 patent are unpatentable under 35 U.S.C. § 103(a) over Kidoguchi, Nakamura, Fujimoto, Shibata, and the Admitted Prior Art.

II. ANALYSIS

A. Claim Construction

We begin our analysis by determining the meaning of the claims. In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech. Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). An inventor may rebut that presumption by providing a definition of the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). In absence of such a definition, limitations are not to be read from

the specification into the claims. *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

1. *"III-V semiconductor" (claim 1); "n-type" as used with semiconductor (claim 1); "pure nitride semiconductor" or "pure nitride compound semiconductor" (claim 12)*

In its petition, Nichia notes that the '215 patent expressly defines these semiconductor claim terms in the specification. Pet. 10-11 (citing Ex. 1001, 5:5-8; 5:14-17; 5:5-12). Upon review of the cited portions of the specification, we observe that the definitions are set forth in the specification with reasonable clarity, deliberateness, and precision. Therefore, we adopt the definitions as the broadest reasonable constructions for the semiconductor claim terms set forth in the table below.

Terms	**Definitions**
III-V semiconductor	A semiconductor according to the stoichiometric formula $Al_a In_b Ga_c N_x As_y P_z$ where (a+b+c) is about 1 and (x+y+z) is also about 1. Ex. 1001, 5:5-8.
"n-type" as used with semiconductor	A semiconductor having n-type conductivity, i.e., a semiconductor in which electrons are the majority carriers. *Id*. at 5:14-17.
Pure nitride semiconductor or pure nitride compound semiconductor	A nitride semiconductor in which x [in the stoichiometric formula $Al_a In_b Ga_c N_x As_y P_z$] is about 1.0. *Id*. at 5:10-12.

2. "annealing" (claim 1)

The claim term "annealing" is recited in claim 1 in the following limitation: "annealing said n-type III-V semiconductor with said stack thereon."

Nichia submits that the claim term "annealing" means "heating to temperatures between 400-900 ºC and for a duration sufficient to cause a desired change in the properties of the contact stack." Pet. 14 (internal quotation marks omitted). We observe that Nichia's construction would import improperly a limitation—"temperatures between 400-900 ºC"—from the specification into the claims. *Van Geuns*, 988 F.2d at 1184. Moreover, Nichia's proposed construction is inconsistent with the specification and the ordinary and customary meaning of the term. For instance, in the background section of the '215 patent discussing prior art methods of forming a contact, there is no indication that the annealing step includes such a temperature-range requirement. Ex. 1001, 1:59-2:10. Therefore, we do not adopt Nichia's proposed construction as the broadest reasonable interpretation for the claim term "annealing."

Emcore urges that the claim term "annealing" should be construed as "heating the semiconductor sufficiently to form a contact with low resistance." PO Resp. 24. In support of its proposed construction, Emcore maintains that "the specification does not require simply any change to occur," but "it requires a specific and beneficial change, i.e., the resulting contact should have a *low resistance and reliable bonding*." PO Resp. 25 (citing Ex. 1001, 4:26-27) (emphasis added). Emcore further argues that

"the method disclosed by the '215 patent emphasizes that it discloses a particular method where annealing a contact with an Al base layer results in a contact with low resistance and reliable boding." PO Resp. 26 (citing Ex. 1011, 4-5). According to Emcore, those statements "distinguishing the claimed invention from the prior art go to the heart of the full understanding of what the inventors actually invented." *Id*. (internal citations omitted).

We do not agree with Emcore that its proposed construction is the broadest reasonable interpretation of the claim term "annealing," as it would import improperly a limitation—"sufficiently to form a contact with low resistance"—from the specification into the claims. *Gemstar-TV Guide Int'l, Inc. v. ITC*, 383 F.3d 1352, 1366 (Fed. Cir. 2004) (rejecting expressly the contention that claims must be construed as limited to an embodiment disclosed in the patent).

We also are not persuaded by Emcore's arguments. They fail to recognize that it is "a bedrock principle of patent law that the claims of a patent define the invention to which the patentee is entitled the right to exclude." *Phillips v. AWH Corp*., 415 F.3d 1303, 1312 (Fed. Cir. 2005) (citations and quotation marks omitted); *see also Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 980 (Fed. Cir. 1995) (en banc) ("The written description part of the specification itself does not delimit the right to exclude. That is the function and purpose of claims.").

Emcore has not alleged that the inventors of the '215 patent acted as their own lexicographer and provided a special definition in the specification for the claim term "annealing" that is different from its recognized meaning

to one with ordinary skill in the art. The claim language used by Emcore is broad. There is no requirement as to the resistivity of the contact or a specific and beneficial change, as urged by Emcore. One with ordinary skill in the art may use "annealing" to form a contact that does not have a low resistance contact or to form other semiconductor structures.

In support of Emcore's position, Dr. Mark S. Goorsky testifies that Emcore's proposed construction is correct, because "[w]hen the '215 patent uses the term 'annealing,' it means specifically a 'contact anneal.'" Ex. 2001 ¶ 61 (citing Ex. 1002 ¶ 31). However, Dr. Goorsky relies on Nichia's expert testimony that does not support Emcore's proposed construction, as it does not discuss Emcore's proposed construction, nor contact resistivity. Ex. 1002 ¶ 31. Neither expert's testimony (Ex. 2001 ¶ 61; Ex. 1002 ¶ 31) explains sufficiently why the term "annealing" should be limited specifically to "heating the semiconductor sufficiently to form a contact with low resistance." As Emcore notes (PO Resp. 25-26), the contacts disclosed in the prior art, including those that are formed with annealing, may or may not produce a low contact resistance. Therefore, Emcore's proposed construction would be inconsistent with the claim term's ordinary and customary meaning as would be understood by one of ordinary skill in the art.

Moreover, Emcore, in its patent owner response, does not explain the meaning of the term "low resistance." PO Resp. 24-26. Upon inquiry at the final oral hearing, counsel of Emcore stated that he agrees with the definition proffered by Nichia's expert, Dr. E. Fred Schubert. Trial Tr. (Paper 66),

34:17-23. Dr. Schubert testifies:

> In 1999-2000, a contact resistance of 10^{-5} Ωcm^2 would simply have reflected the approximate dividing line between a desirable contact and an undesirable contact. Higher than 10^{-5} Ωcm^2 would have been considered a poor contact resistance, while below 10^{-5} Ωcm^2 would have been considered a good contact resistance (for example, Schroder, "Semiconductor Material and Device Characterization," Ex. 1025, p. 125 stated in 1990 that high-quality contacts were on the order of 10^{-6} Ωcm^2). The 1997 review article by Baca, *et al.* surveyed *contacts for n-type III-V semiconductors, and found none that exceeded 10^{-5} Ωcm^2, with most contacts substantially below that value* (Baca, *et al.*, Ex. 1024, p. 604, Table 1).

Ex. 1002 ¶ 55 (emphasis added).

Although that definition of "low resistance" is also consistent with the specification of the '215 patent (Ex. 1001, 4:43-46), Emcore's proposed construction would render the limitation recited in claim 15—"a contact resistance of less than about 10^{-5} ohm-cm^2"—insignificant, if not wholly superfluous. Emcore's proposed construction also would render claim 15, that depends from claim 1, an improper dependent claim under 35 U.S.C. § 112, ¶ 4. Emcore does not explain adequately as to why the term "annealing" recited in independent claim 1 should be construed to require a limitation recited in a dependent claim 15. *Phillips*, 415 F.3d at 1314-15 (stating "the presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim."); *see also Curtiss-Wright Flow Control Corp. v. Velan, Inc.*, 438 F.3d 1374, 1380 (Fed. Cir. 2006) ("In the most specific sense, 'claim differentiation' refers to the presumption that an independent

claim should not be construed as requiring a limitation added by a dependent claim.").

In determining the ordinary and customary meaning of the claim term, it is appropriate to consult a general dictionary definition of the word for guidance. *Comaper Corp. v. Antec, Inc.*, 596 F.3d 1343, 1348 (Fed. Cir. 2010). The ordinary meaning of the word "anneal" includes "to heat (glass, earthenware, metals, etc.) to remove or prevent internal stress."[6]

Consistent with the usage in the prior art and in the specification of the '215 patent, we construe "annealing" as heating the semiconductor structure sufficiently to cause a change in some property of the semiconductor structure. *See e.g.*, Ex. 1001, 1:59-61 ("When the electrode is annealed it becomes transparent so that light emitted within the [light-emitting diodes ("LED")] can pass out of the device through the electrode."); 2:12-15 ("[W]here a gold layer is provided on a contact containing titanium and aluminum, the gold layer can change during annealing."); 4:47-49 ("Where the first barrier layer includes Ti, there can be some diffusion of Ti into the Al-containing base layer during annealing.").

3. "base layer" (claim 1)

Claim 1 recites "depositing Al on the n-type III-V semiconductor to provide a base layer." Emcore submits that the claim term "base layer" should be construed as "[t]he first-deposited metal layer used to form a low-resistance, ohmic contact to the semiconductor." PO Resp. 26-27.

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[6] RANDOM HOUSE WEBSTER'S COLLEGE DICTIONARY (2nd ed. 1999).

We disagree that Emcore's proposed construction is the broadest reasonable interpretation of the claim term "base layer," as it would import improperly a limitation—"a low-resistance, ohmic contact to the semiconductor"—from the specification into the claims.

In support of its position, Emcore cites to Nichia's expert testimony (Ex. 1002 ¶ 20), and the testimony of its expert (Ex. 2001 ¶¶ 62-63), who also cites to Nichia's expert testimony for support of his opinion. However, Nichia's expert testimony does not support Emcore's proposed construction or the opinion of Emcore's expert. As Nichia explains, the portion of Nichia's expert testimony relied upon by Emcore and its expert does not discuss the term "base layer," but rather explains "the function of an ohmic contact layer." Pet. Reply 1; Ex. 1002 ¶ 20.

Further, the background section of the '215 patent (Admitted Prior Art) provides the following:

> In *most semiconductor devices*, the contacts should exhibit "ohmic" characteristics. That is, the electrical voltage loss at the boundary between the contact and the semiconductor material should be substantially proportional to the current, and should be independent of the direction of current flow, so that the contact acts as a conventional electrical resistor. Also, *the contact desirably has low resistance.* For example, a light emitting diode with low resistance ohmic contacts can convert electrical power into light more efficiently than a similar diode with high resistance contacts. The contacts *typically* are connected to metallic leads as, for example, by wire-bonding processes. The contacts should include metals which are [compatible] with these processes.

Ex. 1001, 1:33-46 (emphases added).

As noted in the specification, the goal of forming a low-resistance, ohmic contact is desirable, but not all semiconductor devices have such desirable characteristics. *See also* Ex. 1001, 2:11-20 ("Despite these and other efforts in the art, still further improvements would be desirable."). In light of the specification, we construe the term "base layer" broadly, but reasonably, as "the first-deposited metal layer used to form a contact to the semiconductor."

4. "barrier layer" (claim 1)

Claim 1 recites "depositing Ti on said base layer to provide a first barrier layer" and "depositing Pt on said first barrier layer to provide a second barrier layer." Emcore asserts that the broadest reasonable interpretation of the claim term "barrier layer" is "[a] layer provided to prevent undesirable reactions between the top layer and the base layer." PO Resp. 27 (citing Ex. 1001, 2:53-65; Ex. 1002 ¶ 25).

Upon review of the specification, we observe that Emcore's proposed construction is consistent with the specification and the understanding of one with ordinary skill in the art. Ex. 1001, 2:53-65 ("[I]t is believed that the barrier layers such as Ti and Pt layers above the Al-containing base layer prevent undesirable reactions between Al and the metal of the top layers Au during annealing and/or during service."); Ex. 1002 ¶ 25 ("Barrier layers have the purpose of preventing the diffusion, intermixing, undesirable forms of alloying, and chemical reaction between the first and last deposited metal."). However, the claims require more than one barrier layer.

Therefore, in the light of the claims and specification, we construe the claim term "barrier layer" broadly, but reasonably, as "a layer provided in between two layers to prevent undesirable reactions between the two layers."

B. Obviousness Over Kidoguchi, Nakamura, Fujimoto, Shibata, and the Admitted Prior Art

Nichia asserts that claims 1-17 are unpatentable under 35 U.S.C. § 103(a) over Kidoguchi, Nakamura, Fujimoto, Shibata, and the Admitted Prior Art. Pet. 39. In support of its asserted ground of unpatentability, Nichia provides explanations as to how each limitation is met by the combination of cited prior art references and rationales for combining the prior art references. Pet. 34-47. Nichia also relies upon a declaration of Dr. Schubert. Ex. 1002.

Upon review of Nichia's contentions and supporting evidence, as well as Emcore's patent owner response and supporting evidence, we determine that Nichia has demonstrated, by a preponderance of the evidence, that claims 1-17 of the '215 patent are unpatentable over Kidoguchi, Nakamura, Fujimoto, Shibata, and the Admitted Prior Art.

1. Principles of Law

In an obviousness analysis, it is not necessary to find precise teachings in the prior art directed to the specific subject matter claimed because inferences and creative steps that a person of ordinary skill in the art would employ can be taken into account. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). A basis to combine teachings need not be stated expressly

in any prior art reference. *In re Kahn*, 441 F.3d 977, 987-88 (Fed. Cir. 2006). There need only be an articulated reasoning with rational underpinnings to support a motivation to combine teachings. *Id.* at 988. The level of ordinary skill in the art is reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978).

2. Prior Art

a. Kidoguchi

Kidoguchi describes a method of forming a semiconductor light emitting device. Ex. 1017 ¶ 01. Figure 1 of Kidoguchi is reproduced below:

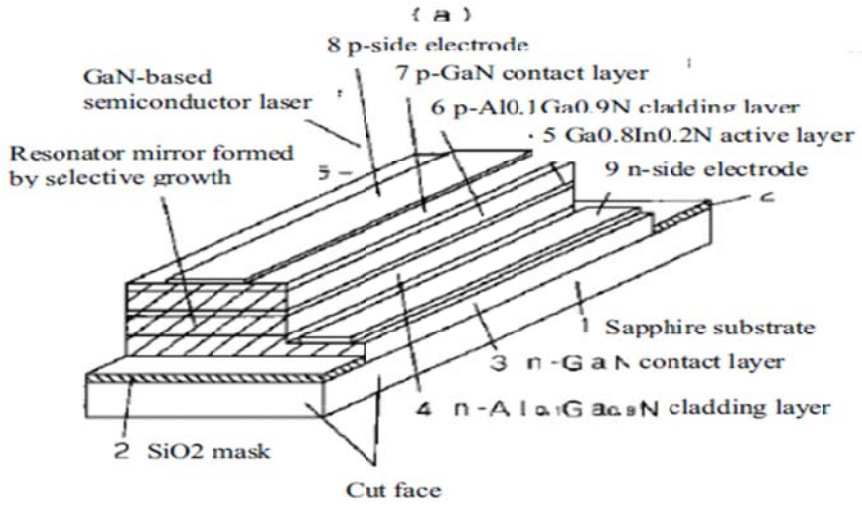

Figure 1 of Kidoguchi depicts the structure of a GaN-based semiconductor laser device formed in accordance with Kidoguchi's invention.

In particular, Kidoguchi discloses forming a GaN-based semiconductor laser device using GaN. Ex. 1017 ¶ 16. Kidoguchi also

discloses forming an n-GaN contact having an electrode that is formed using Ti, Al, and Au, with Au as the outermost layer (i.e., the top layer). *Id*. at ¶ 31. Kidoguchi acknowledges the problem of high contact resistivity and loss of reliability when Au diffuses into the n-type GaN contact layer. *Id*. Kidoguchi teaches a method of suppressing the Au diffusion to decrease the contact resistance. *Id.* at ¶ 32. Kidoguchi's method includes the steps of using Al as the n-GaN contact metal (i.e., the base layer), inserting a Pt layer (i.e., a barrier layer) under the Au layer to suppress the diffusion of Au, and inserting a Ti layer (i.e., a barrier layer) to suppress the diffusion of Pt—to form an Al/Ti/Pt/Au n-side electrode on a GaN semiconductor. *Id*. at ¶¶ 32-33, Fig. 14.

b. Fujimoto

Fujimoto discloses a method of forming GaN semiconductor light emitting devices. Ex. 1007, 1:7-12. Figure 6 of Fujimoto is reproduced below.

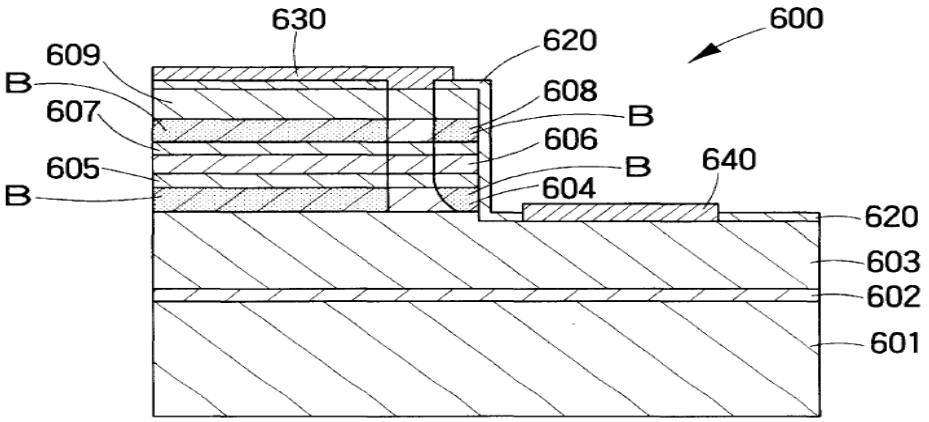

Figure 6 of Fujimoto illustrates a light emitting device formed according to an embodiment of Fujimoto.

As shown in Figure 6 of Fujimoto, semiconductor device 600 has n-side electrode 640 on the n-type GaN semiconductor. Fujimoto discloses forming the electrode with an Al/Pt/Au multi-layered structure and annealing the electrode on the GaN semiconductor at a temperature around 400 ºC. *Id*. at 16:41-46. Fujimoto further teaches interposing one or more Ti layers to the three-layered electrode. *Id*. at 20:13-16.

c. Shibata

Shibata discloses a method of forming a semiconductor light emitting device. Ex. 1019, Abs. Figure 1 of Shibata is reproduced below (emphasis added).

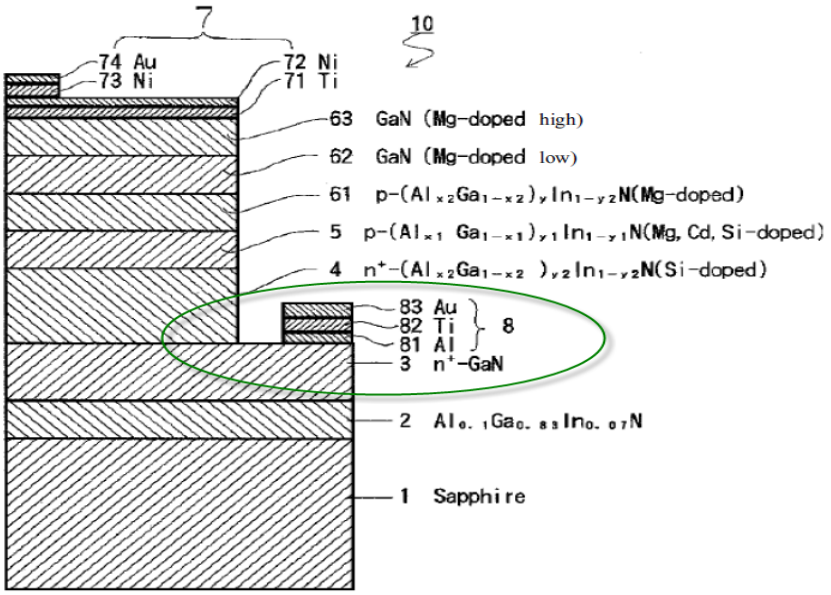

Figure 1 of Shibata shows a cross section of a light emitting device.

As illustrated in Figure 1 of Shibata, light emitting semiconductor device 10 has electrode 8 comprised of an Al/Ti/Au structure formed on n-type GaN semiconductor 3. *Id*. at ¶¶ 11-13, 26. Shibata also describes

annealing the structure at 600 ºC for one minute to form a device with a contact resistance of 10^{-5} ohm-cm^2 or less. *Id*. at ¶ 27. According to Shibata, the resulting device was observed to have sufficient bonding strength and good ohmic contact. *Id*. Shibata also notes other advantages of its invention—extended life of the light emitting device and improved stability of emission. *Id*.

d. Nakamura

Nakamura discloses a method of forming a GaN semiconductor device. Ex. 1013, 1:7-19; 4:43-47. Nakamura notes that, at the time of its invention in the 1994 timeframe, it was known in the art to use Al as a material for an n-electrode of a GaN semiconductor light emitting device. *Id.* at 2:17-19. Nakamura also acknowledges that Al could degrade by an annealing. *Id*. at 2:21-24. Nonetheless, Nakamura describes a method that would overcome that problem by forming a Ti/Al/Au electrode and annealing the structure to establish an ohmic contact to an n-type GaN semiconductor. *Id*. at 2:46-51; 3:19-26; 11:3-14. Nakamura states that annealing at a temperature of 400 ºC or more, for 0.01 to 30 minutes is preferable. *Id*. at 11:15-18.

e. Admitted Prior Art

The Admitted Prior Art includes the background section of the ’221 provisional application (Ex. 1004, 1-2) and the background section of the ’215 patent (Ex. 1001, 1:15-2:9). In particular, the background section of the ’215 patent states that, in most semiconductor devices, the contacts

should exhibit low "ohmic" characteristics and low contact resistance. Ex. 1001, 1:33-40. It also notes that a light emitting diode with low-resistance ohmic contacts can convert electrical power into light more efficiently than a similar diode with high-resistance contacts. *Id*. at 1:40-43. According to the background section of the '215 patent, it was known at the time of the invention to form contacts for n-type GaN by annealing a Ti and Al structure. *Id*. at 1:64-2:4. The background section of the '221 provisional application states that "[t]ypical low work function metal/metal stack with yield low contact resistance to n-GaN on annealing is Al, Ti/Al." Ex. 1004, 1 (emphasis added). It also recognizes that, for the purposes of achieving low contact resistance, "most metallization schemes to n-GaN use Ti, Ti/Al or Al followed by Ni/Au," and "[a]nnealing of the metallization is carried out at temperatures between 400-900 C for minimum contact resistance." *Id*. at 2 (emphasis added).

3. Claims 1 and 11-14

In its patent owner response, Emcore counters that Nichia fails to meet its burden of demonstrating claim 1 of the '215 patent is unpatentable over the combination of Kidoguchi, Nakamura, Fujimoto, Shibata, and the Admitted Prior Art. PO Resp. 32. In particular, Emcore argues that the primary reference Kidoguchi does not describe an Al base layer and barrier layers, as recited in claim 1. Emcore further asserts that the cited prior art references teach away from the claimed invention.

a. Forming Al/Ti/Pt/Au electrode on an n-type GaN semiconductor

Claim 1 requires forming an Al/Ti/Pt/Au structure on an n-type III-V semiconductor. Claims 11 and 12 directly depend from claim 1. Claim 11 further recites "wherein said n-type semiconductor is a nitride compound semiconductor." Claim 12 further recites "wherein said n-type semiconductor is a pure nitride compound semiconductor." Claim 13 depends from claim 11 and further recites "wherein said n-type semiconductor is a gallium nitride based semiconductor." Claim 14 depends from claim 11 and further recites "wherein said n-type semiconductor is GaN." We determine that an *n-type GaN semiconductor* meets the "n-type semiconductor" limitations recited in claims 1 and 11-14.

According to Nichia, Kidoguchi describes an Al/Ti/Pt/Au electrode formed on an n-type GaN semiconductor, as required by claims 1 and 11-14. Pet. 35. Indeed, Figure 14(a) of Kidoguchi shows a contact formed on an n-type GaN semiconductor with layers Mo/Ti/Pt/Au. Kidoguchi discloses that Al can be substituted for Mo because Al is used conventionally for the n-electrode. Ex. 1017 ¶¶ 31-33.

Emcore, however, argues that Kidoguchi does not show an Al base layer. PO Resp. 32-33, 38, 40. Specifically, Emcore alleges that Nichia's English-language translation of Kidoguchi has an error—"conventionally, *Ti and Al are used for the n-side electrode*, but the outermost surface needs to be Au . . . ." (Ex. 1017 ¶ 31, emphasis added). PO Resp. 40. According to Emcore, a proper English-language translation of that sentence—"[a] conventional n-side electrode employs Ti and Al . . ."—shows that the

reference merely discloses Ti/Al/Au as the electrode, and it does not disclose Al as the base layer. PO Resp. 5, 40 (citing Ex. 2011; Ex. 2001 ¶¶ 89-90).

We are not persuaded by Emcore's argument, as it narrowly focus on one sentence and fails to consider Kidoguchi's disclosure as a whole. The alleged translation error also is of no moment. Even based on the English-language translation submitted by Emcore (Ex. 2011), Kidoguchi's disclosure as a whole discloses an embodiment that includes an Al base layer. Ex. 2011 ¶¶ 32-33 ("As illustrated in Figure 14, Mo (molybdenum) is employed as a contact metal for n-GaN. . . . Other metals, however, can be employed instead. For instance, W, Ta, Ti and Al may be employed [as a contact metal for n-GaN]." Emphasis added.). Therefore, Kidoguchi describes an Al base layer formed on an n-type GaN semiconductor, as required by claims 1 and 11-14.

Emcore also argues that Kidoguchi is "a fundamentally flawed lead reference for n-type contacts to GaN and other type III-V semiconductors," because Kidoguchi's primary teaching is a Mo base layer, "which was known not to form a low-resistance, ohmic contact," and Kidoguchi does not explain how other examples of base layer metals could be used to form a low-resistance, ohmic contact. PO Resp. 7-8, 38-39, 41-42.

We are not persuaded by that argument, as it is not commensurate with the scope of claims 1 and 11-14. *See In re Self*, 671 F.2d 1344, 1348 (CCPA 1982) (It is well established that limitations not appearing in the claims cannot be relied upon for patentability.). As discussed above in the claim construction section, we decline to import the limitation—

"a low-resistance, ohmic contact to the semiconductor"—from the specification into the claim term "base layer." Additionally, Emcore does not identify any limitation of claims 1 and 11-14, that expressly requires "a low-resistance, ohmic contact." In fact, the preamble of the sole independent claim, claim 1, merely requires "*forming a contact* on an n-type III-V semiconductor" and not "forming a *low-resistance, ohmic* contact on an n-type III-V semiconductor," as urged by Emcore.

Emcore's argument also fails to recognize that Kidoguchi's disclosure is not limited to the Mo base layer, but also includes the teaching of using Al as the base layer (Ex. 2011 ¶ 33). A prior art reference must be considered for everything it teaches by way of technology and is not limited to the particular invention it is describing and attempting to protect. *EWP Corp. v. Reliance Universal Inc.*, 755 F.2d 898, 907 (Fed. Cir. 1985).

Emcore further asserts that the state of the art at the time of the invention taught that Al was an unsuitable base layer for low-resistance, ohmic contact to n-type GaN. PO Resp. 8, 42. In support of its position, Emcore argues that one with ordinary skill in the art would not have used Al as the base layer in light of Kidoguchi's disclosure, because "its use of Mo as a base layer demonstrates that the intention of [Kidoguchi] was not to create to low-resistance ohmic contact." *Id*. at 8-9, 43.

Emcore's argument is unavailing, as it is not supported by the express teaching of Kidoguchi—Al is used as the base layer on an n-type III-V semiconductor. Ex. 2011 ¶ 33. Moreover, the prior art on record shows that, at the time of the '215 patent's invention, it was known in the art to use

Al as a base layer to form a contact to an n-type III-V semiconductor. *See, e.g.*, Ex. 1004, 1 ("Typical low work function metals/metal stack which yield low contact resistance to n-GaN on annealing is Al, Ti/Al."); Ex. 1007, 16:41-45 (The n-side electrode having a three-layered structure including an Al layer, Pt layer and Au layer, is formed on the n-type GaN contact layer.); Ex. 1019 ¶¶ 11-13, 26 (Light emitting diode 10 has an electrode 8 comprised of an Al/Ti/Au structure formed on an n-type GaN semiconductor.).

For the foregoing reasons, Nichia has demonstrated, by a preponderance of evidence, that the combination of Kidoguchi, Nakamura, Fujimoto, Shibata, and the Admitted Prior Art would have rendered obvious to one with ordinary skill in the art the claim invention, including the "Al" limitation as recited in claims 1 and 11-14.

b. Barrier layers

Claim 1 recites "depositing Ti on said base layer to provide a first barrier layer" and then "depositing Pt on said first barrier layer to provide a second barrier layer." As we discussed above in the claim construction section, we construe the claim term "barrier layer" as "a layer provided in between two layers to prevent undesirable reactions between the two layers."

Emcore argues that Kidoguchi does not disclose the barrier layers of claim 1, because there is no need for barrier layers between a Mo layer and an Au layer. PO Resp. 39-40, 42-43. In particular, Emcore maintains that "Mo is a refractory metal" and "is a candidate for a barrier layer." *Id*. at 39.

Emcore's argument is inapposite, because it again fails to recognize that Kidoguchi discloses an embodiment that does not use Mo as the base

layer, but rather uses an Al base layer. Ex. 2011 ¶¶ 31-33. Moreover, Kidoguchi discloses inserting a Pt layer between the Au top layer and the Al base layer to inhibit excess *Au diffusions* (i.e., preventing undesirable reactions between Au and Al) and to prevent "increases in the contact resistance." Ex. 2011 ¶ 32. Kidoguchi's method also includes a step of inserting a Ti layer between the Pt barrier layer and the Al base layer to suppress *Pt diffusions* (i.e., preventing undesirable reactions between Pt and Al). Ex. 2011 ¶ 32. Given those disclosures of Kidoguchi, we determine that one with ordinary skill in the art at the time of the invention would have appreciated that Kidoguchi's Pt and Ti layers each are barrier layers.

For the foregoing reasons, Nichia has demonstrated, by a preponderance of evidence, that the combination of Kidoguchi, Nakamura, Fujimoto, Shibata, and the Admitted Prior Art would have rendered obvious to one with ordinary skill in the art the claim invention, including the "barrier layers" limitation as recited in claims 1 and 11-14.

c. Annealing

Claim 1 recites "annealing said n-type III-V semiconductor with said stack thereon." Nichia acknowledges that Kidoguchi does not disclose expressly an annealing step. Pet. 35-36. Nevertheless, according to Nichia, annealing a semiconductor with an electrode was known in the art at the time of the invention, to lower the contact resistance of Al contacts to n-type III-V semiconductors. Pet. 39-42. In particular, Nichia cites the following prior art references as support: Fujimoto, Shibata, Nakamura, and the Admitted Prior Art. *Id*. For instance, Nichia notes that Fujimoto describes

annealing an Al/Pt/Au electrode formed on an n-type GaN semiconductor, and that Shibata describes annealing an Al/Ti/Au electrode form on an n-type GaN semiconductor. Pet. 41 (citing Ex. 1007, 16:45-46; Ex. 1019, ¶ 0026-27). As Nichia explains, the Admitted Prior Art states that "annealing of contacts containing Aluminum, Titanium and Gold on n-type GaN (a III-V semiconductor) was known." *Id*. at 40 (citing Ex. 1001, 1:64-2:9). Given the collective teachings of Fujimoto, Shibata, Nakamura, and the Admitted Prior Art, Nichia contends that it would have been obvious to one with ordinary skill in the art at the time of the invention, to anneal Kidoguchi's contact as taught by those prior art disclosures to achieve the desired contact resistance. *Id.* at 41.

Emcore alleges that the cited references teach away from annealing an Al base layer. PO Resp. 43-44. In particular, Emcore argues that "Al was well-known to have problems forming an ohmic contact to n-type GaN and degraded upon annealing." PO Resp. 42. Emcore and its expert attempt to substantiate Emcore's "teaching away" argument by referring to portions of the cited references, e.g., Nakamura, Fujimoto, Shibata, Foresi,[7] and the Admitted Prior Art. PO Resp. 5-6, 33, 42-44, 47-50; Ex. 2001 ¶¶ 99-100.

Nichia counters that the portion of the Admitted Prior art relied upon by Emcore as teaching away from annealing an Al base layer is actually "a warning toward using a diffusion barrier" layer. Pet. Reply 9. Nichia also

[7] Foresi, et al., "Metal contacts to gallium nitride," 62(22) Appl. Phys. Lett. 2859 (31 May 1993) (Ex. 1027).

submits that Emcore fails to recognize that the references "selected Al as a base layer and annealed the contact—despite the alleged fact that the art taught away from using Al as early as 1993." *Id.* at 9-10. Nichia maintains that Nakamura and Foresi are from the early development of GaN-based light emitting devices, but "there was an intense research drive to improve contacts to GaN" between the early and late 1990s. *Id*. at 11. We agree.

"A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the [inventor]." *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994). A reference does not teach away, however, if it merely expresses a general preference for an alternative invention but does not "criticize, discredit, or otherwise discourage" investigation into the invention claimed. *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004).

We are not persuaded by Emcore's arguments and supporting evidence. Instead, we agree with Nichia that a person with ordinary skill in the art, at the time the '215 patent's invention was made, would not have been dissuaded from annealing a contact with an Al base layer. Emcore and its expert erroneously rely upon references, e.g., Nakamura and Foresi, from the early development of GaN-based light emitting semiconductor devices, and fail to discuss meaningfully the state of the art at the time the '215 patent's invention was made. They also narrowly focus on a selected portion of each cited reference, and fail to consider the references in their entirety.

Although the cited references acknowledge the problems associated with annealing an electrode, Emcore and its expert fail to appreciate that the problems noted by the cited references are those that are to be solved by the inventions disclosed in the cited references. For instance, Emcore and its expert focus on a portion in the background section of Fujimoto, and then conclude that Fujimoto teaches away from annealing an Al base layer. PO Resp. 5-6; Ex. 2001 ¶¶ 99-100 (citing Ex. 1007, 2:13-35).

Fujimoto notes that some scientists including Fujimoto's inventors observed difficulties of using Al electrodes. Ex. 1007, 2:20-24. Emcore and its expert, however, fail to take into account that Fujimoto further discloses a method that solves the alleged "annealing" problem. More importantly, Fujimoto teaches annealing a multi-layered electrode—that includes an Al base layer—at a certain temperature range, to form a nitride compound semiconductor light emitting device having a *low contact resistance and good wire bonding*. *Id*. at 2:56-58; 3:53-57. Fujimoto's method includes steps of forming an Al/Pt/Au electrode, and annealing the electrode on the n-type GaN semiconductor at a temperature around 400 ºC. *Id*. at 16:41-46. Fujimoto further teaches inserting one or more Ti barrier layers between the Al and Au layers. *Id*. at 20:13-16. According to Fujimoto, its invention prevents deterioration of electrodes and the light emitting device itself, and significantly improves the reliability of the device. *Id*. at 3:59-62. In light of Fujimoto's disclosure, in its entirety, one with ordinary skill in the art would have understood that the alleged "annealing" problem could have been prevented by using Fujimoto's method of making a nitride compound

semiconductor light emitting device. Therefore, we do not discern that Fujimoto criticizes, discredits, or otherwise discourages annealing an Al base layer.

Emcore and its expert also take the position that Shibata "advises that annealing may cause the contact's top layer to be 'dysfunctional as a bonding pad.'" PO Resp. 5-6 (citing to Ex. 1019 ¶ 28); Ex. 2001 ¶ 45. However, Emcore and its expert fail to consider paragraph 28 of Shibata, as a whole, which discusses the *optimal thicknesses* of the aluminum layer and titanium barrier layer. In fact, Shibata warns against using a titanium barrier layer with a thickness of 1,000 Å or less. Ex. 1019 ¶ 28 ("The optimal thickness of the titanium [barrier] layer 82 is 1,000 Å – 1 μm. If it is 1,000 Å or less, aluminum and gold would react with one another in the [annealing], rendering the layer 83 dysfunctional as a bonding pad."). The purported "annealing" problem is caused by using a barrier layer with a thickness of 1,000 Å or less.

Contrary to Emcore's argument and its expert testimony (PO Resp. 17-19; Ex. 2001 ¶¶ 44-47), Shibata clearly discloses annealing an Al/Ti/Au electrode—that includes an Al base layer—on an n-type GaN semiconductor at 600 °C for one minute to form a light emitting diode with low contact resistance and good ohmic contact. Ex. 1019 ¶ 27. Emcore and its expert (Ex. 2001 ¶ 46) again attempt to substantiate Emcore's position by pointing out a translation or clerical error—"[i]n the above light emitting diode 10, the contact resistance of the aluminum layer 81 relative to the high carrier concentration n+ layer 3 was 10^{-5} Ωcm or less" (Ex. 1019 ¶ 27, emphasis

added). However, one with ordinary skill in the art would have known that "10^{-5} Ωcm" should have been "10^{-5} Ω cm^2" because the unit of measurement for contact resistance is Ω cm^2.

Emcore and its expert further allege that others failed to reproduce the result disclosed in Shibata. PO Resp. 17-19; Ex. 2001 ¶¶ 44-47. Specifically, they direct our attention to the following text in the background section of Fujimoto:

> As a countermeasure against this problem, insertion of Ti as a barrier metal is disclosed in Japanese Patent Laid-Open Publication No 8-274372. However, the Inventors have experimentally found that this approach certainly made wire bonding possible, but invited an increase in contact resistance of the electrode.

Ex. 1007, 2:29-35.

Emcore and its expert, however, did not provide any experimental data regarding the alleged experiment conducted by Fujimoto, e.g., the thicknesses of the metal layers, annealing temperature and time, and contact resistance. Instead, they rely on a vague and ambiguous sentence in the background of Fujimoto.

More importantly, Emcore and its expert ignore the fact that others in the art had reproduced low contact resistance, similar to the results disclosed in Shibata. Notably, Luther[8] reported on a study of Al and Ti/Al contacts to n-type GaN that achieved a low contact resistivity of 8 x 10^{-6} Ω cm^2 and

[8] Luther, et al., "Investigation of the mechanism for Ohmic contact information in Al and Ti/Al contacts to n-type GaN," Appl. Phys. Letters. 70 (1) (6 Jan. 1997) (Ex. 1030, "Luther").

good thermal stability. Ex. 1030, 57 ("Al contacts on *n*-GaN (7×10^{17} cm^{-3}) annealed in forming gas at 600 °C reached a minimum contact resistivity of 8×10^{-6} Ω cm^2 and had much better thermal stability than reported by previous researchers."); *id*. ("[M]any researchers have made Ohmic contacts to *n*-GaN with low contact resistivities . . . ."). Luther's report provides detailed explanation and experimental data, including specific contact resistance as a function of annealing time (Fig. 1) and specific contact resistance as a function of annealing temperature (Fig. 2), e.g., annealing Al contacts to n-GaN between 400 and 600 ºC. *Id*. at 57-59.

Given that Shibata and Luther show that others have achieved low contact resistance and good thermal stability by annealing Al contacts to n-type GaN, the testimony of Emcore's expert—that one of ordinary skill in the art would not have understood Shibata as teaching a low resistance ohmic contact to n-type GaN (Ex. 2001 ¶ 47)—is entitled little weight. *See Velander v. Garner*, 348 F.3d 1359, 1371 (Fed. Cir. 2003) ("In giving more weight to prior publications than to subsequent conclusory statements by experts, the Board acted well with [its] discretion.").

In light of Shibata's disclosure, as a whole, one with ordinary skill in the art at the time of the invention would have understood that (1) using a barrier layer that has an optimal thickness would prevent the purported "annealing" problem, and (2) annealing an Al/Ti/Au electrode on an n-type GaN semiconductor under certain conditions would achieve low contact resistance and good ohmic contact. Therefore, we do not discern that

Shibata criticizes, discredits or otherwise discourages annealing an Al base layer on an n-type GaN semiconductor.

For the foregoing reasons, Nichia has demonstrated, by a preponderance of evidence, that the combination of Kidoguchi, Nakamura, Fujimoto, Shibata, and the Admitted Prior Art would have rendered obvious to one with ordinary skill in the art the claim invention, including the annealing limitation as recited in claims 1 and 11-14.

4. Claims 2-10 and 15-17

a. Thickness of each layer in the Al/Ti/Pt/Au stack

Dependent claims 6-10 and 16-17 require the metal layers to have certain thickness ranges. For instance, claim 6 depends from claim 1, and further recites "wherein said first barrier layer is at least about 300 Å thick." Claim 8 depends from claim 6, and further recites "wherein said deposited Al is between about 190 Å to about 210 Å thick."

Nichia relies upon Shibata and Fujimoto to meet the claimed ranges. Pet. 44-47. In particular, Shibata discloses that a Ti barrier layer that has a thickness of 1,000 Å to 1μm, which falls within the claimed range (at least about 300 Å) of claim 6. Ex. 1019 ¶ 07. Fujimoto discloses a first barrier layer that has a thickness of 50 nm (500 Å), which is close to the claimed range (about 390 Å to about 410 Å) of claim 7. Ex. 1007, 16:42-44; 19:31. Shibata also describes an Al base layer having a thickness of between 100 Å and 1000 Å, which encompasses the claimed range (about 190 Å to about 210 Å) of claim 8. Ex. 1019 ¶ 28. Fujimoto discloses a Pt barrier layer that has a thickness of 500 Å, which falls within the claimed range (about 490 Å

to about 510 Å thick) of claim 9. Ex. 1007, 16:42-44; 18:34-35. Additionally, Shibata discloses an Au top layer having a thickness of 0.5 to 3 μm (5,000 to 30,000 Å), which overlaps the claimed range (at least about 6000 Å) of claim 10. Ex. 1019 ¶ 0028. Shibata further discloses an Al base layer having a thickness of 100 Å and 1000 Å, which encompasses the claim range (about 200 Å) of claim 16, and the claim range (less than about 500 Å) of claim 17.

Notwithstanding that the prior art thicknesses do not fall within all of the claimed ranges, Nichia contends that claims 6-10 and 16-17 are obvious over Kidoguchi, Nakamura, Fujimoto, Shibata, and the Admitted Prior Art. Pet. 44-47. According to Nichia, a person with ordinary skill in the art would have optimized the thickness of each layer to prevent undesirable diffusion, and to achieve the desired contact resistance and wire bonding properties. *Id*. Notably, as Nichia observes, Kidoguchi provides that the function of a barrier layer is to prevent excessive diffusion of Au and Pt, and to lower the contact resistance (Ex. 1017 ¶ 32). Pet. 44-45. That function depends on the thickness of the layers. *Id*.

Emcore counters that Nichia's asserted ground of unpatentability is based on impermissible hindsight. In particular, Emcore alleges that "a barrier layer's ability to prevent diffusion is not solely dependent on the thickness of the barrier layer." PO Resp. 56 (citing Ex. 2001 ¶¶ 109-111). Emcore contends that "there are many rules and relationship[s] that must be considered" including "how the barrier layer relates to the other layers in the resulting contact." *Id*. Emcore argues that this relationship between the

layers for a GaN semiconductor is present only in the '215 patent. *Id*. at 56-57 (citing Ex. 1001, 4:36-40 ("The Al thickness decides the thickness of the other layers. As Al thickness increases, it is necessary to increase the thickness of the Ti and Pt layers to avoid diffusion of Al into Au and diffusion of Au into Al.").

We are not persuaded by Emcore's arguments and expert's testimony. Rather, we determine that one with ordinary skill in the art at the time of the '215 patent's invention would have recognized that, in light of the cited prior art references, the thickness of each metal layer in an electrode is a result effective variable. In that regard, it is well established that "discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art." *In re Boesch*, 617 F.2d 272, 276 (CCPA 1980); *In re Antonie*, 559 F.2d 618, 620 (CCPA 1977).

Emcore's argument and its expert testimony (Ex. 2001 ¶¶ 110-111) are based on the erroneous premise that the prior art must provide the exact method of optimization, as the one disclosed in the '215 patent, for the variable to be result-effective. However, as our reviewing court noted, "the prior art need not provide the exact method of optimization for the variable to be result-effective." *In re Applied Materials, Inc.*, 692 F.3d 1289, 1297 (Fed. Cir. 2012). "A recognition in the prior art that a property is affected by the variable is sufficient to find the variable result-effective." *Id*.

On the record before us, the prior art shows that the thickness of each barrier layer affects the reduction of metal diffusions between the layers. Notably, Shibata discloses that if the titanium barrier layer is less than a

certain thickness, aluminum and gold will react with one another in the annealing step, rendering the Au layer dysfunctional as a bonding pad. Ex. 1019 ¶ 28. Kidoguchi also teaches that the function of the barrier layers is to prevent diffusion of Pt and Au. Ex. 2011 ¶ 32. Moreover, Fujimoto discloses that the Pt layer prevents the top and base layers "from mixing, and maintains them operative for their intended" purposes. Ex. 1007, 18:43-45.

Shibata further recognizes that the thickness of the Al base layer affects the reaction between the Au top layer and the Al base layer, and also affects whether an ohmic contact would be achieved. Ex. 1019 ¶ 28. Shibata teaches that the thickness of the Au top layer affects the length of time for forming the layer, the bonding performance, and the cost of making the device. *Id*. Given those prior art teachings, one with ordinary skill in the art would have appreciated that the thickness of each metal layer in the electrode is a result-effective variable.

We also have reviewed the parties' supporting evidence, and we credit the testimony of Nichia's expert over the testimony of Emcore's expert. *Yorkey v. Diab*, 601 F.3d 1279, 1284 (Fed. Cir. 2010) (finding Board has discretion to give more weight to one item of evidence over another "unless no reasonable trier of fact could have done so"). We find the explanations proffered by Nichia's expert to be more consistent with the prior art teachings discussed above. In particular, Nichia's expert, Dr. Schubert, testifies that "the prior art references indicate that the barrier layers are effective, which would have motivated a person of ordinary skill to use those thicknesses." Ex. 1002 ¶ 69 (citations omitted) (citing Ex. 1019 ¶ 28;

Ex. 1007, 18:43-45); *see also* Ex. 1002 ¶¶ 44-50. Dr. Schubert further testifies that one of ordinary skill in the art would have the skill set to optimize the thickness of the Al base layer to sufficiently form an ohmic contact with the underlying semiconductor. Ex. 1002 ¶¶ 44-45, 50-51, 71. Additionally, Dr. Schubert declares that one with ordinary skill in the art would have used the thickness described in Shibata (Ex. 1019 ¶¶ 0009, 0012, 0027) to facilitate wire bonding. Ex. 1002 ¶ 69.

Emcore's expert, Dr. Goorsky, narrowly focuses on one sentence in Dr. Schubert's declaration and concludes that Dr. Schubert's testimony is misleading. Ex. 2001 ¶ 109 (citing Ex. 1002 ¶ 50). Dr. Goorsky does not explain meaningfully why the prior art cited by Dr. Schubert in his testimony does not support his statement, e.g., "the prior art has many examples of first barrier (Ti) layers thicker than 300 Å, for example Murarka, et al., p. 158, Table I and Vandenberg, et al., p. 3677, Table I" (Ex. 1002 ¶ 48); and "[t]he interactions between the metals on either side of the Ti and Pt barriers were known, for example, from Murarka, *et al.*" (Ex. 1002 ¶ 50).

Accordingly, Nichia has demonstrated, by a preponderance of evidence, that it would have been obvious to one with ordinary skill in the art to optimize the thickness of each metal layer in the electrode stack to prevent undesirable diffusion, and to achieve the desire contact resistance and wire bonding properties.

b. Annealing temperature and time; contact resistance

Dependent claims 2-5 recite certain annealing conditions, e.g., time and temperature. For instance, claim 2 depends from claim 1, and further recites "wherein said annealing step is performed at about 400-600 °C," and claim 3 depends from claim 2, and further recites "wherein said annealing step is performed for between about 1 minute and about 10 minutes."

Claim 15 depends from claim 1 and is the only claim that imposes a limitation requiring a contact resistance—"wherein said Al/Ti/Pt/Au contact has a contact resistance of less than about 10^{-5} ohm-cm^2."

Nichia relies upon Kidoguchi, Nakamura, Fujimoto, Shibata, and the Admitted Prior Art to meet the claimed ranges. Pet. 43-44, 46. In particular, Fujimoto discloses an annealing temperature of around 400 ºC, which is within the claimed range (400-600 ºC) of claim 2. Ex. 1007, 16:45-46. Shibata discloses an annealing step that performs at 600 ºC for one minute, which is within the claimed range (about one minute to about 10 minutes) of claim 3. Ex. 1019 ¶ 27. Nakamura discloses an annealing step that performs at 400 ºC or more for 0.01 to 30 minutes, which encompasses the claimed value (about three minutes) of claim 4. Ex. 1013, 11:14-18. Nakamura also discloses an annealing temperature of 500 ºC, as recited in claim 5. *Id*. at 11:65-12:1.

Notwithstanding that the prior art thicknesses do not fall within all of the claimed ranges, Nichia contends that claims 2-5 and 15 would have been obvious over Kidoguchi, Nakamura, Fujimoto, Shibata, and the Admitted Prior Art. Pet. 43-44, 46. According to Nichia, one with ordinary skill in

the art would have optimized the annealing temperature and time to achieve a contact resistance of about 10^{-5} ohm-cm^2 or lower in light of the prior art. Pet. 43, 46. As support, Nichia submits a declaration of Dr. Schubert (Ex. 1002), and directs our attention to the '215 patent, which provides that "[m]oderate temperatures of 400-600 C are sufficient for low contact resistances of 10^{-5} Ωcm^2 or lower." Pet. 46 (citing Ex. 1001, 4:43-46) (internal quotation marks omitted).

Dr. Schubert testifies that the annealing temperature and time would have been optimized readily to achieve the desired contact resistance. Ex. 1002 ¶¶ 52-54, 67. Specifically, Dr. Schubert observes that annealing Kidoguchi's contact as suggested by Nakamura, Fujimoto, Shibata, and the background section of the '221 provisional application would have achieved a contact resistance of 10^{-5} Ωcm^2. *Id*. ¶¶ 55, 70.

Emcore disagrees and argues that the cited prior art references do not disclose a method of obtaining a contact resistance of 10^{-5} Ωcm^2 or lower using an Al base layer. PO Resp. 58. As to claims 2-5, Emcore relies upon the arguments directed to independent claim 1, and proffers no additional arguments. *Id*. at 55.

We are not persuaded by Emcore's argument. Rather, we agree with Nichia that one with ordinary skill in the art at the time of the '215 patent's invention would have optimized the annealing temperature and time to achieve the desired contact resistance of 10^{-5} Ω cm^2. As discussed above, Shibata clearly discloses annealing an Al/Ti/Au electrode—that includes an Al base layer—on an n-type GaN semiconductor at 600 °C for one minute to

form a light emitting diode with good ohmic contact and low contact resistance of 10^{-5} Ω cm^2 or lower. Ex. 1019 ¶ 27.

It is well established that "discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art." *Boesch*, 617 F.2d at 276; *Antonie*, 559 F.2d at 620. In that regard, a "recognition in the prior art that a property is affected by the variable is sufficient to find the variable result-effective." *Applied Materials*, 692 F.3d at 1297. The prior art of record shows that the annealing conditions of an Al base layer to an n-type GaN semiconductor are result-effective variables, as they are recognized by the prior art to achieve good ohmic contact and low contact resistance. Notably, the Admitted Prior Art expressly states that "[a]nnealing of the metallization is carried out at [a] temperature between 400-900 C for minimum contact resistance." Ex. 1004, 2. Shibata also recognizes that annealing an n-type GaN semiconductor with an electrode having a base Al layer at 600 C for one minute would yield a light emitting diode with good ohmic contact and low contact resistance of 10^{-5} Ω cm^2. Ex. 1019 ¶ 27; *see also* Ex. 1030, Figs 1-2 (showing specific contact resistance as a function of annealing time and temperature). Therefore, the annealing temperature, annealing time, and contact resistance are result-effective variables.

Accordingly, Nichia has demonstrated, by a preponderance of evidence, that it would have been obvious to one with ordinary skill in the art to optimize the annealing temperature, annealing time, and contact resistance to achieve the desired contact resistance and good ohmic contact.

5. Secondary Considerations of Nonobviousness

Factual inquiries for an obviousness determination include secondary considerations based on evaluation and crediting of objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). Notwithstanding what the teachings of the prior art would have suggested to one with ordinary skill in the art at the time of the '215 patent's invention, the totality of the evidence submitted, including objective evidence of nonobviousness, may lead to a conclusion that the claimed invention would not have been obvious to one with ordinary skill in the art. *In re Piasecki*, 745 F.2d 1468, 1471-1472 (Fed. Cir. 1984). Secondary considerations may include any of the following: long-felt but unsolved needs, failure of others, unexpected results, commercial success, copying, licensing, and praise. Here, Emcore argues that its claimed method "overcame the failure of others and achieved the unexpected result of making a contact with Al base layer that has surprisingly low resistance of 10^{-5} ohm-cm^2 or better." PO Resp. 52 (citing Ex. 2001 ¶ 105).

Failure of Others

Emcore asserts that many others "tried and failed to make a suitable ohmic contact using Al as a base layer to n-type GaN." *Id*. at 52; *see id*. at 14-20. In support of that assertion, Emcore submits that the research "by Nichia and Dr. Nakamura in 1993 led them to conclude that aluminum 'can hardly establish an ohmic contact with the n-type gallium nitride-based III-V Group compound semiconductor layer, and [tend] to degrade by [an]

annealing treatment, losing the electrical conductivity,'" and Nakamura (Ex. 1013) concluded that "Al led to poor wire bonding with top wire." *Id*. at 52-53 (citing Ex. 1013, 2:20-25). Emcore further maintains that Foresi "revealed that using Al as a base layer to n-type GaN resulted in contacts with poor contact resistance and that the contact resistance of Al-based contact increased upon annealing." *Id*. at 53 (citing Ex. 1027). Emcore also relies upon its expert testimony (Ex. 2001 ¶¶ 35-52). *Id*. at 14-20.

Nichia disagrees and responds that there were others who had used Al as a base layer to n-type GaN successfully before the '215 patent, e.g., Shibata, Fujimoto, and Luther. Pet. Reply 9-10, 13. Nichia also argues that nonobviousness cannot be established unless the claimed invention is the first to solve the problem that caused the failure. *Id*. (citing *Graham*, 383 U.S. at 36.). We agree.

Emcore's argument and supporting evidence (Ex. 2001 ¶¶ 35-52) narrowly focus on the early development of GaN-based light emitting semiconductor devices, e.g., the research conducted by Nichia and Dr. Nakamura in 1993, and Foresi published in 1993. As to the 2000 timeframe, Emcore and its expert merely rely upon the background of the '221 provisional application (the Admitted Prior Art), which provides:

> Annealing of the metallization is carried out at temperatures between 400-900 C for minimum contact resistance. However, this annealing is accompanied by degradation in the surface morphology, *due to metallurgical reactions between the metal layers* in the stack. This causes difficulty in subsequent *wire bonding* in devices and results in potential device failure during service.

PO Resp. 20; Ex. 2001 ¶ 52; Ex. 1004, 2 (emphasis added). As noted by Nichia, the portion of the '221 provisional application relied upon by Emcore and its expert is "a warning toward using a diffusion barrier" layer. Pet. Reply 9. That purported "failure" is similar to the aforementioned problem noted in Shibata to warn against using a Ti barrier layer that has a thickness less than the optimal range (Ex. 1019 ¶ 28). As discussed above, Shibata and Fujimoto disclose methods of solving the aforementioned problems associated with annealing an Al base layer. Notably, Shibata discloses an ohmic contact using Al as a base layer to n-type GaN that has a low contact resistance of 10^{-5} Ω cm^2 or less. Furthermore, others in the art have formed Al contacts to n-type GaN and achieved low contact resistance (e.g., 8 x 10^{-6} Ω cm^2) and good thermal stability (Ex. 1030). The inventors of the '215 patent, therefore, are not the first to solve the problem of using Al as a base layer to n-type GaN, and they are not the first to achieve a low contact resistance of 10^{-5} Ω cm^2 or less.

For the foregoing reasons, the objective evidence, as to failure of others, proffered by Emcore is insufficient to establish nonobviousness.

Unexpected Results

Emcore argues that the claimed method of the '215 patent "achieved an unprecedented combination of low contact resistance, good thermal stability and excellent wire bonding for an Al-based contact to n-type GaN" and "generated unexpected benefit of using Al as a base layer to increase the efficiency of LED." PO Resp. 50-51, 53. Emcore takes the position that the inventors of the '215 patent have "achieved the unexpected result of making

a contact with Al base layer that has surprisingly low resistance of 10^{-5} Ωcm^2 or better." *Id*. at 52. To support its position, Emcore relies upon its expert's testimony. *Id*. at 54 (citing Ex. 2001 ¶¶ 105-108).

To be of relevance, evidence of nonobviousness must be commensurate in scope with the claimed invention. *In re Tiffin*, 448 F.2d 791, 792 (CCPA 1971) (evidence of success for cups is not commensurate in scope with containers). In order to be accorded substantial weight, there must be a nexus between the merits of the claimed invention and the evidence of secondary considerations. *GPA*, 57 F.3d at 1580. "Nexus" is a legally and factually sufficient connection between the objective evidence and the claimed invention, such that the objective evidence should be considered in determining nonobviousness. *Demaco Corp. v. F. Von Langsdorff Licensing Ltd.*, 851 F.2d 1387, 1392 (Fed. Cir. 1988). The burden of showing that there is a nexus lies with the patent owner. *In re Paulsen*, 30 F.3d 1475, 1482 (Fed. Cir. 1994); *Demaco Corp.*, 851 F.2d at 1392.

We are not persuaded by Emcore's argument and evidence, as they fail to establish a nexus between the merits of the claimed invention and the asserted unexpected results.

Claims 1-14 and 16-17 do not recite a contact resistance, much less a low contact resistance of 10^{-5} Ωcm^2. According to Emcore and Dr. Goorsky, the claimed feature to which the asserted unexpected results links is the use of *Al as a base layer*. PO Resp. 50-55; Ex. 2001 ¶¶ 105-108.

Contrary to Emcore's argument and expert testimony, the inventors of the '215 patent are not the first in the art to use an Al base layer on an n-type GaN semiconductor. As discussed above, at the time of the '215 patent's invention, others in the art had achieved similar results with an Al base layer. *See, e.g.*, Ex. 1019; Ex. 1030. Where the offered secondary consideration actually results from something other than what is both claimed and novel in the claim, there is no nexus to the merits of the claimed invention. *Tokai Corp. v. Easton Enters., Inc.*, 632 F.3d 1358, 1369 (Fed. Cir. 2011) ("If commercial success is due to an element in the prior art, no nexus exists."); *see also Ormco Corp. v. AlignTechnology, Inc*., 463 F.3d 1299, 1312, 1313 (Fed. Cir. 2006) ("[I]f the feature that creates the commercial success was known in the prior art, the success is not pertinent." Reasoning that success that is due "'partially' to claimed features" and to unclaimed features and/or other features already in the art lacks the requisite nexus to show unobviousness.) (citations omitted). In the absence of an established nexus with the claimed invention, secondary consideration factors are entitled little weight, and generally have no bearing on the legal issue of obviousness. *See In re Vamco Machine & Tool, Inc.*, 752 F.2d 1564, 1577 (Fed. Cir. 1985). Accordingly, Emcore's objective evidence is accorded little weight.

Further, Emcore and its expert testimony fail to make a showing of unexpected results—a showing that the claimed invention exhibits some superior property or advantage that one of ordinary skill in the art would have found surprising or unexpected. *See In re Soni*, 54 F.3d 746, 750 (Fed.

Cir. 1995). As we discussed above, Shibata discloses *annealing an Al base layer* at 600 °C and for one minute to form a light emitting diode. Ex. 1019 ¶ 27. More importantly, Shibata discloses the same "unexpected results" as asserted by Emcore and its expert testimony (PO Resp. 50-53; Ex. 2001 ¶¶ 105-108)—a light emitting diode that has good thermal stability, good ohmic contact, good wire bonding, as well as low contact resistance of 10^{-5} Ω cm^2 or lower. Ex. 1019 ¶ 27. Notably also, Luther discloses *annealing Al contacts* to achieve ohmic contacts, low contact resistivity of 8×10^{-6} Ω cm^2, and good thermal stability. Ex. 1030, 57 ("Al contacts on *n*-GaN (7×10^{17} cm^{-3}) annealed in forming gas at 600 °C reached a minimum contact resistivity of 8×10^{-6} Ω cm^2 and had much better thermal stability than reported by previous researchers."); *id*. ("[M]any researchers have made Ohmic contacts to *n*-GaN with low contact resistivities . . . ."). Given those prior art disclosures, one with ordinary skill in the art would not have found an n-type Al contact with a contact resistivity of a 10^{-5} Ω cm^2 surprising or unexpected.

Emcore further asserts that the claimed method is praised by Nichia. PO Resp. 54-55 (citing Ex. 2001 ¶ 55). Emcore directs our attention to Yoneda,[9] in which Nichia allegedly stated that "it is preferable to use an Al/Ti/Pt/Au or Al/Ti/Au because it efficiently reflects light and, therefore, increases the light extraction efficiency of an LED." *Id*. at 53-54 (citing Ex. 2001 ¶¶ 105-108; Ex. 2004 ¶¶ 138-139). Dr. Goorsky also relies upon

[9] Yoneda, Pub. No. US 2012/0273823 (Nov. 1, 2012) (Ex. 2004).

Yoneda as evidence that "there is a strong relation (or nexus) between the merits of the claimed invention of the '215 patent (e.g. claim 1) and these secondary considerations of nonobviousness." Ex. 2001 ¶ 106 (citing Ex. 2004 ¶¶ 136-139). Although Yoneda expresses a preference of using an Al/Ti/Pt/Au or Al/Ti/Au electrode (Ex. 2004 ¶¶ 137-139), such evidence is not sufficient to establish a nexus between Emcore's claimed method and the alleged unexpected result. Emcore and Dr. Goorsky's testimony do not show sufficiently that Yoneda is referring specifically to the claimed method of the '215 patent. As discussed above, it was known in the art at the time of '215 patent's invention to use an Al/It/Pt/Au electrode. Yoneda could have been referring to other prior art teachings, including Kidoguchi (Ex. 1017 ¶¶ 31-32) and Kawamura (Ex. 1015 ¶ 15) which disclose using an Al/Ti/Pt/Au electrode on an n-type semiconductor. Emcore and its expert testimony do not provide sufficient explanation how a preference of using an Al/Ti/Pt/Au electrode is linked to Emcore's claimed method specifically. Therefore, the mere fact that Yoneda prefers an Al/Ti/Pt/Au electrode does not support a showing of unexpected result, nor establishes a nexus between the merits of the claimed invention and the asserted unexpected results.

Emcore further asserts that the claimed method is used by Nichia. PO Resp. 54-55 (citing Ex. 2001 ¶ 55). Dr. Goorsky declares that "Nichia's 219 series products have used the contact of the claimed invention from at least 2011 to the present." Ex. 2001 ¶ 55 (citing Exs. 2012, 2013). Even assuming that Nichia uses an Al base layer in its products, that does not add sufficiently to the record to warrant a conclusion of nonobviousness,

because, as we indicated previously, an Al base layer was known in the art at the time of the '215 patent's invention. *See In re Baxter Travenol Labs*, 952 F.2d 388, 392 (Fed. Cir. 1991) (finding the prior art possessed the function relied upon by the patent applicant to establish unexpected results and, therefore, was not a basis for rebutting a prima facie finding of obviousness.); *J.T. Eaton & Co., Inc. v. Atlantic Paste & Glue Co.*, 106 F.3d 1563, 1571 (Fed. Cir. 1997) ("[T]he asserted commercial success of the product must be due to the merits of the claimed invention beyond what was readily available in the prior art.").

Dr. Eliashevich, one of the named inventor of the '215 patent, also testifies that "the contact of claim 1 was incorporated into hundreds of thousands of LEDs that were sold." Ex. 2025 ¶ 18; Ex. 2002 ¶ 18. However, Dr. Eliashevich's testimony is not sufficient to support nonobviousness of claim 1, because Dr. Eliashevich's testimony does not establish adequately that the sales of hundreds of thousands of LEDs constitutes commercial success when considered in relation to overall market share. Dr. Eliashevich does not provide any data pertaining to overall market share, and there is no indication that LED sales number represents a substantial quantity in the overall market share. *See In re Baxter Travenol*, 952 F.2d at 392 ("Information solely on numbers of units sold is insufficient to establish commercial success.").

After weighing the evidence of obviousness and nonobviousness of record, on balance, we conclude that the strong evidence of obviousness outweighs the weak evidence of nonobviousness. For the foregoing reasons,

we determine that Nichia has demonstrated that claims 1-17 are unpatentable under 35 U.S.C. § 103(a) over Kidoguchi, Nakamura, Fujimoto, Shibata, and the Admitted Prior Art.

C. Motion to Amend

Emcore filed a motion to amend claims. Paper 26, "Mot. A." Emcore requests to cancel claims 2-5, 7-9, 12, 16, and17 of the '215 patent, and replace the cancelled claims with proposed new claims 18-27. *Id*. at 1. For the reasons stated below, Emcore's motion to amend claims is *denied.*

An *inter partes* review is more adjudicatory than examinational, in nature. *See Abbott Labs v. Cordis Corp*., 710 F.3d 1318, 1326 (Fed. Cir. 2013). A motion to amend claims in an *inter partes* review is not itself an amendment. As the moving party, Emcore bears the burden of proof to establish that it is entitled to the relief requested. 37 C.F.R. § 42.20(c). In sum, Emcore's proposed substitute claims are not entered automatically, but only upon Emcore having demonstrated the patentability of those substitute claims.

1. A reasonable number of substitute claims

In a motion to amend, a patent owner may, for each challenged claim, propose a reasonable number of substitute claims. 35 U.S.C. § 316(d)(1). The presumption is that only one substitute claim would be needed to replace each challenged claim, although the presumption may be rebutted by a demonstration of need. 37 C.F.R. § 42.121(a)(3). Absent special circumstances, a challenged claim can be replaced by only one claim, and a

motion to amend should, for each proposed substitute claim, specifically identify the challenged claim that it is intended to replace. Each proposed claim should be traceable to an original challenged claim as a proposed substitute for that claim.

Here, Emcore's motion to amend claims indicates that all of the proposed claims are new claims. Mot. A. 1-3. Emcore generally identifies the challenged claims, as a group, to be cancelled and identifies the proposed new claims, as a group. *Id*. Emcore fails to demonstrate which proposed new claim is replacing which specific challenged claim. None of the proposed new claims are traceable to any challenged claims. In other words, the motion fails to identify the challenged claim that a specific proposed substitute claim is intended to replace. Without such indication, the Board does not have adequate information to determine the reasonableness of the number of substitute claims for each original claim. Furthermore, Emcore improperly proposes an independent substitute claim, claim 22, without cancelling an independent challenged claim.

For the foregoing reasons, Emcore's motion to amend fails to present a reasonable number of substitute claims in violation of 37 C.F.R. § 42.121(a)(3).

2. Claim listing

A motion to amend claims must include a claim listing that clearly identifies the changes, so that new limitations and deletions of limitations can be identified easily and quickly. 37 C.F.R. § 42.121(b). However, Emcore's motion to amend presents a claim listing that contains inaccurate

information. More specifically, Emcore's claim listing identifies only one limitation, as a new limitation, without identifying other new limitations and deletions of limitations. Mot. A. 1-3. For instance, Emcore fails to identify the limitation in proposed claim 18—"wherein the top layer prevents cratering of the semiconductor during bonding"—as a new limitation, and fails to identify the limitation in claim 2—"wherein said annealing step is performed at about 400-600 ºC"—as a deletion. *Id*. The inaccuracy in the claim listing causes unnecessary delay. The burden should not be placed on the Board to sort through Emcore's patent claims and proposed claims to determine which limitations are added and which limitations are eliminated.

Without proper identification of all of the changes, Emcore's motion to amend claims fails to comply with 37 C.F.R. § 42.121(b).

3. Claim construction

Claim construction is an important step in a patentability determination. *Oakley, Inc. v. Sunglass Hut Int'l,* 316 F.3d 1331, 1339 (Fed. Cir. 2003); *Medichem, S.A. v. Rolabo, S.L.*, 353 F.3d 928, 933 (Fed. Cir. 2003) ("Both anticipation under § 102 and obviousness under § 103 are two-step inquiries. The first step in both analyses is a proper construction of the claims. . . . The second step in the analyses requires a comparison of the properly construed claim to the prior art.") (internal citations omitted).
A motion to amend claims must identify how the proposed substitute claims are to be construed, especially when the proposed substitute claims introduce new claim terms.

Here, Emcore's proposed substitute claims introduce several new claim terms including "*cratering* of the semiconductor during *bonding*" (*see* proposed new claim 18, emphasis added), and "the top layer has a *surface morphology* which permits *reliable bonding*" (*see* proposed new claim 20, emphasis added). Mot. A. 1-3. Although Emcore proffers constructions for claim terms, "annealing," "base layer," and "barrier layer" that are recited in the challenged claims, Emcore does not provide any constructions for the new claim terms recited in its proposed substitute claims. *Id*. at 3-4. For example, the claim term "reliable bonding" is a relative term, Emcore does not provide any explanation as to how one with ordinary skill in the art would have determined whether a bonding is reliable or not, or identify whether the specification sets forth a special definition.

Without a proper construction of the new claim terms, Emcore's motion does not provide adequate information for the Board to determine whether Emcore has demonstrated the patentability of its proposed substitute claims, and thus, Emcore fails to meet its burden of proof under 37 C.F.R. § 42.20(c).

4. The Amendment Must Respond to a Ground of Unpatentability

Pursuant to 35 U.S.C. § 316(a)(9) and taking into account the statutory considerations under 35 U.S.C. § 316(b)—"the effect of any such regulation on the economy, the integrity of the patent system, the efficient administration of the Office, and the ability of the Office to timely complete proceedings instituted"—the Office promulgated 37 C.F.R. § 42.121 to set forth the standards and procedures for allowing a patent owner, in an *inter*

partes review, to move to amend the patent "to cancel a challenged claim or propose a reasonable number of substitute claims." As set forth in 37 C.F.R. § 42.121(a)(2), a motion to amend may be denied where the amendment does not respond to a ground of unpatentability involved in the trial.

In Emcore's motion, all of the features of original challenged claims 2-5, 7-9, 12, 16, and 17 are being removed, including the temperature range that is said to produce the asserted "unexpected result" of low contact resistances of 10^{-5} ohm-cm^2. Mot. A. 1-3. For instance, none of Emcore's proposed substitute claims recites the temperature ranges, annealing time ranges, and base layer thickness ranges recited in those challenged claims, e.g., "said annealing step is performed at about 400-600 ºC" (claim 2); "said annealing step is performed for between about 1 minute and about 10 minutes" (claim 3); and "said base layer is about 20 nm thick" (claim 16). *Id*. at 1-3.

Emcore does not explain adequately why the removal of all those limitations is responsive to a ground of unpatentability. Emcore fails to appreciate that a patent owner may not seek to broaden a challenged claim in any respect, in the name of responding to a ground of unpatentability. A proposed substitute claim is not responsive to a ground of unpatentability of a challenged claim if it removes any feature of the challenged claim being replaced, and even more so, as here, if all of the features of the challenged claim are being removed.

By eliminating the features of the challenged claims being replaced, Emcore's motion to amend claims fails to comply with 37 C.F.R. § 42.121(a)(2).

5. Written Description Support

A motion to amend claims must identify clearly the written description support for each proposed substitute claim. 37 C.F.R. § 42.121(b)(1). The written description test is whether the original disclosure of the application relied upon reasonably conveys to a person of ordinary skill in the art that the inventor had possession of the claimed subject matter as of the filing date. *Ariad Pharms., Inc. v. Eli Lilly & Co.,* 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc). Therefore, the written description support must be shown in the original disclosure of the application that issued as the patent.

Here, Emcore fails to provide any citation to the original disclosure of the application, Application No. 09/971,965 ("the '965 application") that issued as the '215 patent. More specifically, Emcore's motion to amend does not cite to the originally-filed specification of the '965 application for the actual claim language of each proposed substitute claim. Although Emcore cites to the '215 patent, that alone is insufficient. For instance, Emcore provides a citation, without any explanation, to the patent claims that may or may not be a part of the original disclosure—"Proposed claim 21: *See, e.g.* existing claims 6, 14, and 15." Mot. A. 5. Such a vague statement is inadequate to determine the written description support for Emcore's proposed substitute claims. The burden should not be placed on

the Board to sort through Emcore's patent and the original disclosure of the '965 application to determine whether each proposed substitute claim is supported in the original disclosure of the '965 application.

For the foregoing reasons, Emcore's motion to amend fails to set forth the written description support for each proposed substitute claim, in violation of 37 C.F.R. § 42.121(b)(1).

6. Patentability over Prior Art

An *inter partes* review is neither a patent examination proceeding nor a patent reexamination proceeding. The proposed substitute claims, in a motion to amend, are not entered automatically and then subjected to examination. Rather, the proposed substitute claims will be added directly to the patent, without examination, if the patent owner's motion to amend claims is granted. The patent owner is not rebutting a rejection in an Office Action, as though this proceeding is a patent examination or a reexamination. Instead, the patent owner bears the burden of proof in demonstrating patentability of the proposed substitute claims over the prior art in general, and thus entitlement to add these proposed substitute claims to its patent.

A mere conclusory statement (*see, e.g.*, Ex. 2001 ¶ 112) that one or more added claim features are not described in any prior art or would not have been suggested or rendered obvious by the prior art is facially inadequate. It also is insufficient for Emcore simply to explain why the proposed substitute claims are patentable in consideration of the ground of unpatentability on which the Board instituted review. Mot. A. 11-15.

Emcore's motion to amend does not discuss all of the references on record, e.g., Kawamura (Ex. 1015). Further, relying on its expert testimony on the validity of claim 1—a claim that does not recite any of the new features added in the proposed substitute claims—is inapposite. Mot. A. 6 (citing Ex. 2001 ¶¶ 67-104). In fact, with respect to the proposed substitute claims, Dr. Goorsky merely testifies:

> I have analyzed the claims set forth in Emcore's Motion to Amend. In light of the foregoing, it is my opinion that those claims are valid and nonobvious over the prior art of Ground 4 [—the ground of unpatentability on which the Board instituted review].

Ex. 2001 ¶ 112.

Dr. Goorsky's declaration does not discuss each new feature added in the proposed substitute claims. Neither Emcore's motion, nor Dr. Goorsky's testimony, discusses the level of ordinary skill in the art, explaining the basic knowledge and skill set already possessed by one of ordinary skill in the art, with respect to the new claim features. Limiting the discussion to the references relied upon in the instituted ground of unpatentability does not provide a meaningful analysis.

Without having discussed sufficiently the prior art references on the record, the level of ordinary skill in the art, and what was known previously regarding the new claim features, Emcore fails to demonstrate the patentability of the proposed substitute claims.

7. Conclusion

For the foregoing reasons, Emcore has not, in its motion, set forth a prima facie case for the relief requested or satisfied its burden of proof. Consequently, consideration of Nichia's opposition and Emcore's reply is unnecessary.

D. Nichia's Motion to Exclude

Nichia seeks to exclude: (1) Emcore's evidence related to the commercial success of Nichia's 219 products (Ex. 2001 ¶ 55; Ex. 2012; Ex. 2013); (2) Dr. Goorsky's statements regarding the relevance of unexamined Japanese Patent Applications (Ex. 2001 ¶ 89); and (3) Dr. Ivan Eliashevich's supplemental declaration (Ex. 2025 ¶ 6) and the file history of the '215 patent (Ex. 2026, 5-28). Paper 46 ("Mot."). As the movant, Nichia has the burden of proof to establish that it is entitled to the requested relief. 37 C.F.R. § 42.20(c).

With regard to Emcore's evidence related to the commercial success of Nichia's 219 products (Ex. 2001 ¶ 55; Ex. 2012; Ex. 2013), Nichia argues that Emcore has not shown that Nichia's 219 products embody any claim of the '215 patent, and that any evidence of commercial success of Nichia's 219 products are irrelevant. Mot. 3. Pursuant to Rules 802 and 603 of the Federal Rules of Evidence, Nichia alleges that Dr. Goorsky's underlying test results are inadmissible hearsay, and the underlying test results are statements that were not made under oath. Mot. 3-4. As to Dr. Goorsky's statements regarding the relevance of unexamined Japanese Patent

Applications, Nichia asserts that Dr. Goorsky, who has no legal expertise in Japanese patent applications, is "not qualified to offer expert opinions about the impact of Japanese patent procedures on the level of scrutiny to which Japanese patent applications are subjected." Mot. 5-6. Nichia further asserts that Dr. Eliashevich's supplemental declaration (Ex. 2025 ¶ 6) and the file history of the '215 patent (Ex. 2026, 5-28) are improper papers because they attempt to correct deficiencies in Emcore's Motion to Amend. Mot. 7-8.

Even without excluding Emcore's evidence, we have determined that Nichia has demonstrated, by a preponderance of the evidence, that claims 1-17 of the '215 patent are unpatentable.

Accordingly, Nichia's motion to exclude is *dismissed* as moot.

E. Emcore's Motion to Exclude

Emcore seeks to exclude the following: (1) certain portions of Dr. Schubert's second declaration (Ex. 1035) filed in support of Nichia's opposition to Emcore's motion to amend; and (2) Nichia's document filed in the related district court litigation (Ex. 1036). Paper 49 ("PO Mot."). As the movant, Emcore has the burden of proof to establish that it is entitled to the requested relief. 37 C.F.R. § 42.20(c). For the reasons set forth below, Emcore fails to meet its burden, and therefore, Emcore's motion to exclude is *denied*.

Testimony on Patent Law and Sufficiency of the Evidence

Emcore alleges that certain portions of Dr. Schubert's second declaration (Ex. 1035 ¶¶ 14-16, 17-19, 33, 39, 44, 47, 51) should be

excluded because Dr. Schubert testified to the ultimate issue of patent law. PO Mot. 1, 6-9. Emcore also asserts that certain portions of Dr. Schubert's second declaration (Ex. 1035 ¶¶ 33, 39, 44, 47, 51) should be excluded, as Dr. Schubert did not read at least one reference and ignored teachings of other references. PO Mot. 9-12. Nichia relies upon Dr. Schubert's second declaration in its opposition (Paper 40) to Emcore's motion to amend claims (Paper 26).

We are not persuaded by Emcore's arguments. There is a strong public policy for making all information filed in a non-jury, quasi-judicial administrative proceeding available to the public, especially in an *inter partes* review which determines the patentability of claims in an issued patent. It is better to have a complete record of the evidence submitted by the parties than to exclude particular pieces.

We recognize that expert testimony on the ultimate "legal conclusion of obviousness is neither necessary nor controlling." *Avia Grp. Int'l, Inc. v. L.A. Gear Cal., Inc*., 853 F.2d 1557, 1564 (Fed. Cir. 1988). It is within the Board's discretion to assign the appropriate weight to be accorded to evidence. In its motion, Emcore has not explained adequately why the Board should exclude expert testimony on patent law or testimony that does not have adequate support, instead of giving it little or no weight. *See, e.g.*, *Donnelly Garment Co. v. NLRB*, 123 F.2d 215, 224 (8th Cir. 1942) ("One who is capable of ruling accurately upon the admissibility of evidence is equally capable of sifting it accurately after it has been received . . . ."). Moreover, Emcore may not challenge, in a motion to exclude, the

sufficiency of the evidence. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48765, 48767 (Aug. 14, 2012). The Board is capable of taking into account the baselessness of a witness's testimony, if any, when weighing all of the testimony of the witness.

For the foregoing reasons, we decline to exclude any portion of Dr. Schubert's second declaration (Ex. 1035).

Nichia District Court Filing (Ex. 1036)

Emcore seeks to exclude the Notice Correcting Corporate Names (Ex. 1036) that was filed in the district court litigation, because it is irrelevant, potentially prejudicial, and inadmissible hearsay. PO Mot. 12-15. We are not persuaded by Emcore's arguments.

As discussed previously, Emcore, in its patent owner response, alleged that Nichia failed to identify all real parties-in-interest in its petition. PO Resp. 1. As support, Emcore submitted a copy of Nichia's motion to stay (Ex. 2017) to show that Nichia represented to the district court that both Nichia Corporation and NAC filed the petition in the instant proceeding. *Id*. at 2 (citing Ex. 2017, 1). In response to Emcore's allegation, Nichia countered that its motion to stay contained a clerical error, and filed a copy of the Notice Correcting Corporate Name (Ex. 1036)—to establish that Nichia has notified the district court of the clerical error made in its motion to stay.

Upon review of the parties' evidence (Ex. 2017; Ex. 1036), we determine that there is little, if any, prejudice to Emcore. The Notice Correcting Corporate Name (Ex. 1036) is merely a paper filed in the district

court to notify the district court of a clerical error. A complete record of the evidence submitted by the parties is necessary to preserve the file history of this proceeding. Contrary to Emcore's argument, the notice is not hearsay, because it a public document and was submitted merely to show that Nichia has notified the district court of the clerical error. Furthermore, it is relevant to the real party-in-interest issue raised by Emcore.

For the foregoing reason, we decline to exclude Nichia's Notice Correcting Corporate Name (Ex. 1036).

No New Arguments or Sur-reply

While a motion to exclude may raise issues related to admissibility of evidence, it is not an opportunity for submitting new arguments or a sur-reply. Here, Emcore, in its motion to exclude, introduces new arguments that should have presented in its patent owner response, and arguments that amount to an improper sur-reply. PO Mot. 7-13.

Notably, for the first time, Emcore specifically presents, in its motion to exclude, an argument regarding the *commercial success* of its claimed method, and identifies specific portions of the evidence that support that argument. *Id*. at 7-9. Although Emcore submits arguments for secondary considerations of nonobviousness concerning failure of others and unexpected results of its claimed method, no "commercial success" argument was presented in Emcore's patent owner response. PO Resp. 50-55. The term "commercial success" does not appear even in Emcore's patent owner response. *Id*. It is unreasonable for Emcore to contend that Nichia's expert fails to consider Emcore's "commercial success" argument

and evidence. In fact, Emcore itself fails to present that argument and supporting evidence in its patent owner response.

In its motion to exclude, Emcore alleges that it presented, in its patent owner response, evidence of secondary considerations of nonobviousness that includes: (1) "Nichia's use of the '215 patent resulted in a *commercial success* of Nichia's 219 products;" and (2) Dr. Eliashevich's testimony that the contact of the '215 patent "was incorporated into '*hundreds of thousands of LEDs that were sold*.'" PO Mot. 7 (citing to Ex. 2001 ¶ 55; Ex. 2025 ¶ 18) (emphases added). However, Emcore did not cite to Dr. Eliashevich's declaration (Ex. 2025; Ex. 2002), nor provide any specific explanation as to the commercial success of its claimed method in the "Secondary Considerations" section of its patent owner response. PO Resp. 50-55. In fact, the entire patent owner response does not cite to the particular paragraph (Ex. 2025 ¶ 18; Ex. 2002 ¶ 18) of Dr. Eliashevich's declaration that is said to be supporting Emcore's alleged "commercial success" argument.

Emcore also fails to present the portion of Dr. Goorsky's declaration (Ex. 2001 ¶ 55) that purportedly supports its "commercial success" argument, in an unambiguous manner. Emcore cites, in a *footnote*, to Dr. Goorsky's declaration (Ex. 2001 ¶ 55), which merely repeats the same vague and general statements made in Emcore's patent owner response. PO Resp. 54. The purported analysis on Nichia's 219 products (Exs. 2012 and 2013) is not cited in Emcore's patent owner response, but in a *footnote* of Dr. Goorsky's declaration (Ex. 2001 ¶ 55). Citing evidence in a footnote and

incorporating by reference other evidence within an expert declaration creates confusion, and violates the page limit. *Cf. Globespanvirata, Inc. v. Tex. Instruments, Inc.*, 2005 WL 3077915, *1 (D. N.J. 2005) (Defendants provided cursory statements in motion and sought to make its case through incorporation of expert declaration and a claim chart. Incorporation by reference of argument not in motion was held to be a violation of local rules governing page limitations and was not permitted by the court).

All arguments supporting the patentability of Emcore's patent claims should have been made in the patent owner response, in a reasonably unambiguous manner, to give Nichia a fair opportunity to reply and avoid inefficiency, cost, and unnecessary delays. Otherwise, it is prejudicial to Nichia, circumvents the Board's rules, and impacts the Board's ability to complete the proceeding timely. *See, e.g.,* 35 U.S.C. § 316(b).

The patent owner response itself must identify and explain specific portions of the evidence that support arguments for the patentability of the patent claims. The Board may give no weight to the evidence where a patent owner has failed to state its relevance or to identify specific portions of the evidence that support the patent owner's arguments. Emcore should not expect the Board to search the record and piece together what may support Emcore's arguments. *Cf.*, *DeSilva v. DiLeonardi*, 181 F.3d 865, 866-67 (7th Cir 1999) ("A brief must make all arguments accessible to the judges, rather than ask them to play archaeologist with the record.").

III. CONCLUSION

Nichia has met its burden of proof, by a preponderance of the evidence, in showing that claims 1-17 of the '215 patent are unpatentable under 35 U.S.C. § 103(a) over Kidoguchi, Nakamura, Fujimoto, Shibata, and the Admitted Prior Art.

Emcore has not met its burden that its proposed substitute claims are patentable.

IV. ORDER

In consideration of the foregoing, it is

ORDERED that claims 1-17 of the '215 patent are *cancelled*;

FURTHER ORDERED that Emcore's Motion to Amend Claims is *denied*;

FURTHER ORDERED that Nichia's Motion to Exclude Evidence is *dismissed*; and

FURTHER ORDERED that Emcore's Motion to Exclude Evidence is *denied*.

Case IPR2012-00005
Patent 6,653,215

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US006653215B1

(12) **United States Patent**
Brown et al.

(10) **Patent No.: US 6,653,215 B1**
(45) **Date of Patent: Nov. 25, 2003**

(54) **CONTACT TO N-GAN WITH AU TERMINATION**

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(73) Assignee: **Emcore Corporation**, Somerset, NJ (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/971,965**

(22) Filed: **Oct. 5, 2001**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/692,953, filed on Oct. 20, 2000.
(60) Provisional application No. 60/238,221, filed on Oct. 5, 2000.

(51) **Int. Cl.**[7] **H01L 21/28**; H01L 21/3205
(52) **U.S. Cl.** **438/600**; 438/604; 438/605; 438/606; 438/48
(58) **Field of Search** 438/604–606, 438/46, 933, 752, 597; 257/613, 615, 616, 91, 99, 103, 744, 745, 600

(56) **References Cited**

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Lin et al., "Low Resistance Ohmic Contacts on Wide Bank Cap GaN," 64(8) Applied Physics Letters, Feb. 1994, pp. 1003–1005.

* cited by examiner

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(57) **ABSTRACT**

A contact for n-type III–V semiconductor such as GaN and related nitride-based semiconductors is formed by depositing Al,Ti,Pt and Au in that order on the n-type semiconductor and annealing the resulting stack, desirably at about 400–600° C. for about 1–10 minutes. The resulting contact provides a low-resistance, ohmic contact to the semiconductor and excellent bonding to gold leads.

17 Claims, 2 Drawing Sheets

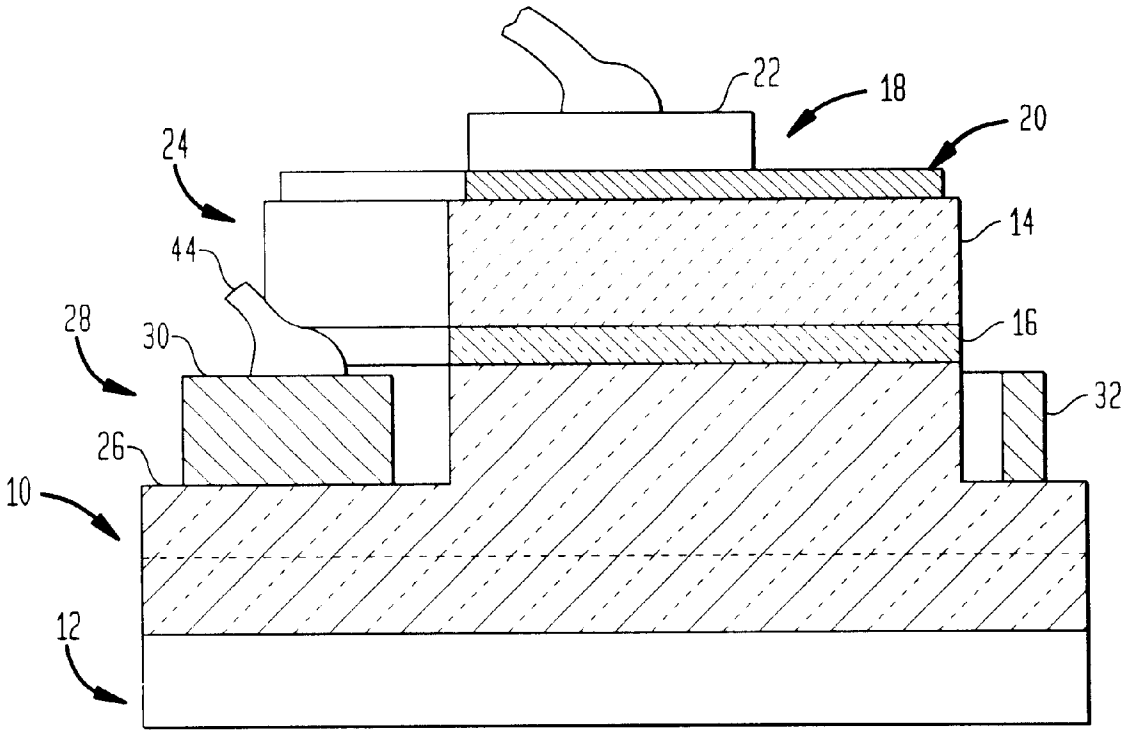


FIG. 1

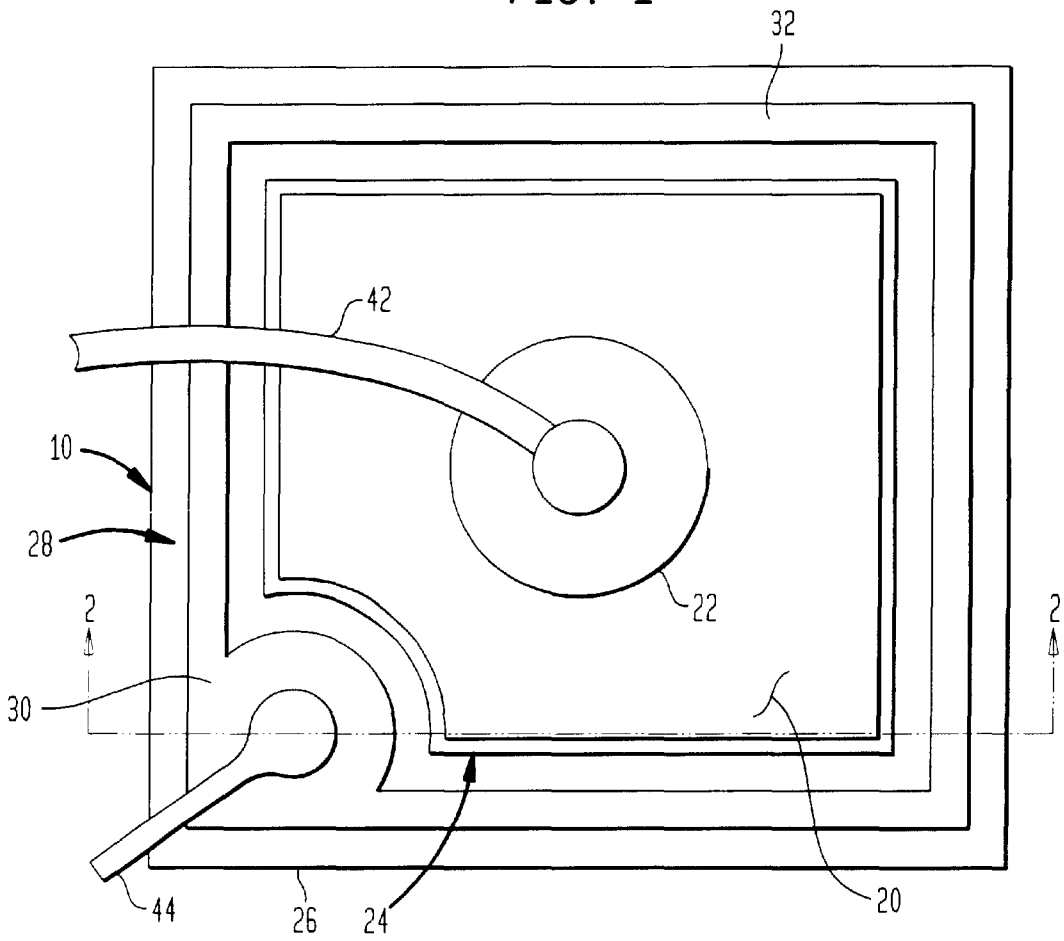


FIG. 2

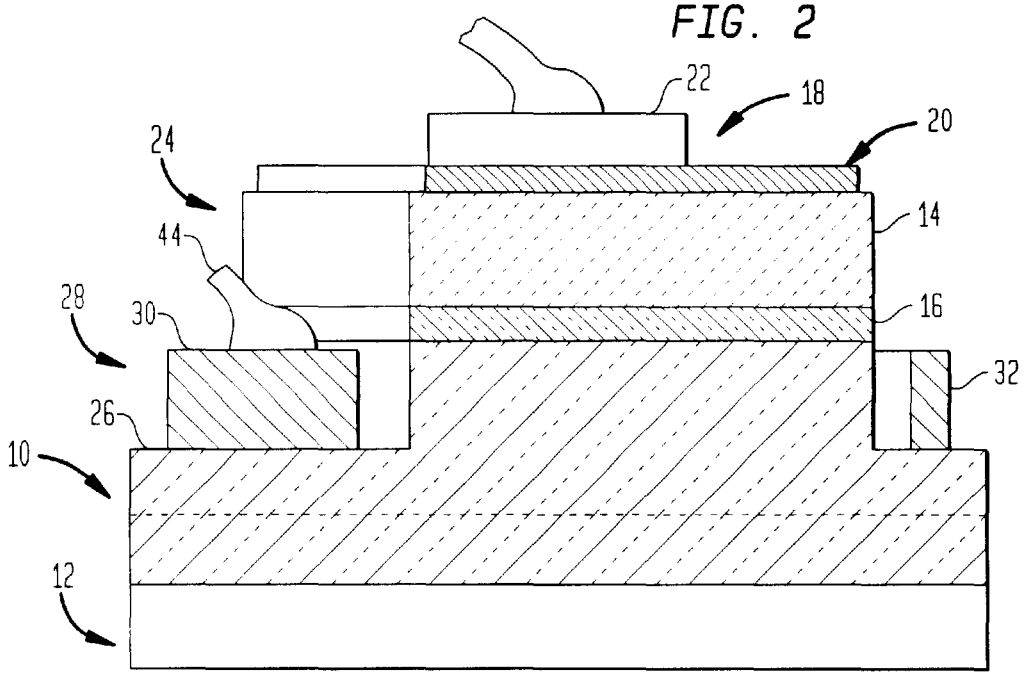
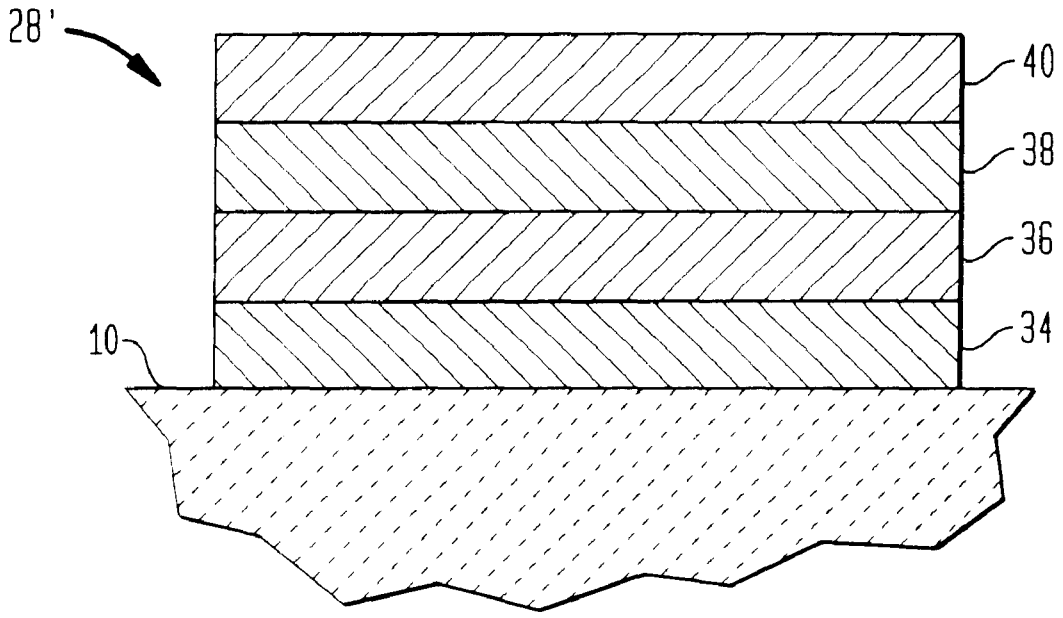


FIG. 3



CONTACT TO N-GAN WITH AU TERMINATION

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application claims benefit of U.S. Provisional Patent Application No. 60/238,221, filed Oct. 5, 2000, the disclosure of which is hereby incorporated by reference herein. The present application is also a continuation-in-part of U.S. patent application Ser. No. 09/692,953 Oct. 20, 200, the disclosure of which is hereby incorporated by reference herein.

BACKGROUND OF THE INVENTION

Typical semiconductor devices include regions of material having n-type conductivity, in which electrical current is carried principally by electrons, and material having p-type conductivity, in which electrical current is carried principally by electron vacancies, commonly referred to as "holes." The semiconductor device is connected to an external electical circuit by contacts. For example, a light-emitting diode includes p-type and n-type regions and a junction between these regions. A contact referred to as the p-contact is provided on the p-type region, whereas a contact referred to as the n-contact is provided on the n-type region. When an electrical voltage in the proper direction is applied between these contacts by an external power source, a current flows between the contact. Electrons in the n-type region and holes in the p-type region move toward the junction and combine with one another at or adjacent to the junction to produce light.

In most semiconductor devices, the contacts should exhibit "ohmic" characteristics. That is, the electrical voltage loss at the boundary between the contact and the semiconductor material should be substantially proportional to the current, and should be independent of the direction of current flow, so that the contact acts as a conventional electrical resistor. Also, the contact desirably has low-resistance. For example, a light emitting diode with low-resistance ohmic contacts can convert electrical power into light more efficiently than a similar diode with high-resistance contacts. The contacts typically are connected to metallic leads as, for example, by wire-bonding processes. The contacts should include metals which are compatable with these processes.

The materials which provide low-resistance ohmic contacts vary with the composition and conductivity type of the semiconductor in the device. Certain semiconductor devices are formed from III–V materials, i.e., compounds of formed from a material in Group III of the periodic table and a material in Group V of the periodic table as, for example, gallium nitride (GaN) and similar materials. Contacts for p-type GaN commonly include gold or combinations of gold and nickel. For example, contacts for use on light-emitting diodes commonly include an electrode formed from thin layers of gold and nickel abutting the p-type GaN and a thick pad region including a layer of gold at the top surface of the pad. When the electrode is annealed it becomes transparent so that light emitted within the LED can pass out of the device through the electrode. The gold-containing pad provides a surface suitable for wire bonding using gold wires. The pad covers only a small portion of the device surface.

Lin et al., *Low Resistence Ohmic Contacts On Wide Band Gap GaN*, 64 (8) Applied Physics Letters February 1994, at 1003–1005, and U.S. Pat. No. 5,563,422 disclose contacts for n-type GaN formed from titanium, aluminum, or both, which is annealed. The '422 patent states that if titanium and aluminum are provided in a multi-layer structure, deposition of titanium should be performed first, followed by deposition of aluminum. A contact including only titanium and aluminum would be incompatable with gold wire bonding. Accordingly, the '422 patent suggests covering the Ti/Au structure with a "high-melting point metallic material" preferably including gold as a topmost layer, and preferably including another high-melting metal such as titanium and/or nickel.

Despite these and other efforts in the art, still further improvements would be desirable. For example, where a gold layer is provided on a contact containing titanium and aluminum, the gold layer can change during annealing. These changes impair the reliability of the wire bonds. It would be desirable to provide a contact and contact-forming method for n-type GaN and other n-type III–V semiconductors which would provide a low-resistance ohmic contact and which would also allow reliable bonding of gold leads such as gold wires to the contact.

SUMMARY OF THE INVENTION

One aspect of the invention provides a method of forming a contact on an n-type III–V semiconductor comprising the steps of depositing a base layer formed predominantly from Al on an n-type III–V semiconductor; then depositing a first barrier layer formed predominantly of one or more first barrier metals selected from the group consisting of Ti,Ta and Pd on the base layer; then depositing a second barrier layer formed predominantly of one or more second barrier metals selected from the group consisting of Pt, W and alloys of Ti and W on said first barrier layer. The method according to this aspect of the invention further includes the step of depositing a top layer formed predominantly of one or more top metals selected from the group consisting of Au and Ag on said second barrier layer, whereby said layers form a stack on the n-type semiconductor.

The deposited layers form a stack on the n-type semiconductor. The n-type III–V semiconductor with the stack is annealed to form the contact.

The III–V semiconductor preferably is a "nitride semiconductor," i.e. a III–V semiconductor in which N constitutes 50% or more, and preferably 80% or more of the group V element. The semiconductor more preferably is a gallium nitride based semiconductor, i.e., a nitride semiconductor including gallium as, for example, GaN, InGaN, AlGaN or AlInGaN. The annealing step typically is performed at a temperature of about 400–600° C. for about 1–10 minutes. Most preferably, the base layer consists essentially of Al, the first barrier layer consists essentially of Ti, the second barrier layer consists essentially of Pt and the top layer consists essentially of Au.

Although the present invention is not limited by any theory of operation, it is believed that the barrier layers such as Ti and Pt layers above the Al-containing base layer prevent undesirable reactions between Al and the metal of the top layer Au during annealing and/or during service. Although the present invention also is not limited by any theory of operation in this respect as well, it is believed that the Al in the base layer abutting the n-type semiconductor diffuses into the semiconductor and/or forms intermediate materials at the boundary with the n-type semiconductor. Whatever the mechanism of operation, the resulting contact has a low resistance and ohmic behavior. There may be some alloying of Ti and Al, and/or some alloying of Pt and Au.

A further aspect of the present invention provides a semiconductor unit including n-type III–V semiconductor

with an n-type contact made as discussed above. The unit may further include a lead, preferably a gold-containing lead such as a gold wire or a gold-covered lead formed from another material, bonded to the contact.

These and other objects, features and advantages of the present invention will be more readily apparent from the detailed description of the preferred embodiments set forth below, taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagrammatic top plan view of a semiconductor unit in accordance with one embodiment of the present invention.

FIG. **2** is a sectional view taken along line **2**—**2** in FIG. **1**.

FIG. **3** is a diagrammatic sectional view of a portion of the unit illustrated in FIG. **2**, during one stage of a process in accordance with one embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A semiconductor unit in accordance with one embodiment of the invention is a light-emitting diode having a semiconductor body including an n-type III–V semiconductor region **10** formed on a substrate **12**, a p-type semiconductor region **14** and a junction **16** between the p-type and n-type regions. A p-contact **18** includes a thin transparent electrode **20** overlying the surface of the p-type region **14** and a bonding pad **22** covering a relatively small portion of the electrode. The p-contact may be of conventional structure and may include, for example, gold and nickel in the electrode **20** and gold in the pad **22**. The semiconductor body defines a mesa portion **24** projecting upwardly from a ledge **26**. The ledge **26** is defined by the n-type region **10**, so that the ledge surface constitutes a surface of the n-type region. As best seen in FIG. **1**, ledge **26** extends around the periphery of mesa **24**, and the ledge has an enlarged region at one corner of the semiconductor body. An n-contact **28** includes a relatively wide, circular pad region **30** and a thin, elongated striplike region **32** extending along the edge region and encircling the mesa portion. As described in greater detail in the aforementioned U.S. patent application Ser. No. 09/692,953, this physical configuration of the electrodes promotes spreading of the electrical current throughout the horizontal extent of the device (in the directions parallel to the plane of the drawing in FIG. **1**).

Contact **28** is formed by a multilayer deposition process. As seen in FIG. **3**, contact **28'** is in an in-process state prior to the annealing operation discussed below. The contact in this state is also referred to as a "stack" of layers. In this in-process state, the contact of this embodmient includes a base layer **34** abutting the n-type semiconductor **10**, a first barrier layer **36** overlying the base layer, a second barrier layer **38** overlying the first barrier layer, and a top layer **40** overlying the second barrier layer and forming the top or exposed surface of the contact, remote from the n-type semiconductor.

The base layer desirably consists essentially of aluminium, with or without some titanium. The first barrier layer should be formed predominantly from one or metals selected from the group consisting of titanium, tantalum and palladium, and preferably consists essentially of one of these metals. Most preferably, the first barrier layer consists essentially of titanium. The second barrier layer should be formed from one or more metals selected from the group consisting of platinum, tungsten or alloys of tungsten and titanium. Preferably, the second barrier layer consists essentially of one of these metals. Most preferably, the second barrier layer consists essentially of platinum. The top layer should be formed predominantly of one or more metals selected from the group consisting of gold or silver, and preferably consists essentially of gold or silver. As used in this disclosure, the expression "formed predominantly of" a metal means that the layer includes at least about 75% of such metal. Each of these layers may include minor amounts of impurities which do not materially affect the performance of the finished contact as discussed below. The base layer in the in-process contact, before anneal may include substantial amounts of Ti, as, for example, up to about 25%. In this case, the step of depositing Al can include the step of depositing some Ti along with the Al. Preferably, each layer in the in-process contact, prior to annealing, consists essentially of a single metal as recited, and is as close to a pure, single metal layer as practicable. Layers **34**–**40** may be deposited by essentially any conventional deposition technique which does not contaminate the underlying semiconductor or other elements of the device incorporating the semiconductor, as, for example, sputtering, evaporation, and plating.

After deposition, layers **34**–**40** constituting the in-process contact or stack are annealed. Annealing is required from a low resistance contact. Although the present invention is not limited by any theory of operation, it is believed that the mechanism involves diffusion of Al through the native oxide on n-GaN, to intimate contact with the n-GaN. It is believed that layera **36** and **38** substantially prevent reaction between Al and Au or Ag in the top layer during annealing.

One typical stack or in-process contact includes about 190–210 Å of aluminum, about 390–410 Å of titanium, about 490–510 Å of platinum and about to 6000 Å to 5 μm of gold. These thicknesses can be varied. The Al thickness decides the thickmess of the other layers. As Al thickness increases, it is necessary to increase the thickness of the Ti and Pt layers to avoid diffusion of Al into Au and diffusion of Au into Al. With increased thickness of Au, the possibility of cratering of the semiconductor during wire bonding dramatically reduces.

The annealing of this stack can be performed either in nitrogen, argon or other inert gas, or air. Moderate temperatures of 400–600 C. are sufficient for low contact resistances of the order of 10^{-5} ohm-cm^2 or lower. A preferred annealing process is conducted at 500° C. for 3 minutes in air. Where the first barrier layer includes Ti, there can be some diffusion of Ti into the Al-containing base layer during annealing. Where the top layer is formed predominantly from Au and the second barrier layer is formed predominantly from Pt, the finished contact **28**, at the end of the annealing process, has a top surface portion which consists essentially of the Au, but which may include some Pt. Most preferably, this surface portion is essentially devoid of Al, and preferably is essentially devoid of Ti as well.

After annealing, the resulting semiconductor unit may be connected to gold-bearing leads such as fine gold wires **42** and **44** by bonding the leads to the pad **22** of the p-contact and to the pad portion **30** of the n-contact. The bonding process may be performed using conventional wire-bonding equipment. The surface morphology of the annealed n-contact is excellent, and correspondingly, the adhesion of the wire bond to the contact is excellent. This is evidenced by the nonobservation of any failure of the wire bond at the bond/contact interface during wire bond stress tests. The failure always occurs at the ball/wire interface.

Although the invention has been described above with reference to n-type GaN, it can also be applied to form contacts on other n-type III–V semiconductors, most preferably nitride semiconductors and pure nitride semiconductors. As used in this disclosure, the term "III–V" semiconductor means a semiconductor according to the stoichiometric formula $Al_aIn_bGa_cN_xAs_yP_z$ where (a+b+c) is about 1 and (x+y+z) is also about 1. The term "nitride semiconductor" refers to a III–V semiconductor in which x is 0.5 or more, most typically about 0.8 or more. The term "pure nitride semiconductor" refers to a nitride semiconductors in which x is about 1.0. The term "gallium nitride based semiconductor" as used herein refers to a nitride semiconductor including gallium. The term "n-type" as used herein with reference to a semiconductor means a semiconductor having n-type conductivity, i.e., a semiconductor in which electrons are the majority carriers. Certain semiconductors, such as GaN, exhibit n-type conductivity even when undoped. n-type conductivity can be imparted or enhanced by addition of conventional dopants as, for example, Si. Typically, the n-type semiconductor and the contact formed according to the invention is incorporated in a device which also includes other semiconductors. For example, the device may be an optoelectronic device such as a laser or light emitting diode ("LED") which includes a p-type semiconductor and a p-n junction between the p-type semiconductor and the n-type semiconductor.

It is not essential to provide all of the layers over the entire surface area of the in-process n-contact **28**'. For example, in the configuration illustrated in FIGS. **1** and **2**, only the pad region **30** of the finished n-contact **28** is bonded to a lead **44**. Thus, the Au or other top layer **40** and the Pt or other second barrier layer **38** may be omitted in portions of the in-process contact which will form the strip region **32**.

The particular contact configuration illustrated in FIG. **1** is only illustrative. The same contact forming process and contact metallurgy can be applied in to formation of an n-contact of any size or shape. Leads other than gold wires can be bonded to the contacts. For example, the leads can be provided as parts of lead frames or on dielectric supports of the types commonly used in tape automated bonding ("TAB") processes. Further, the semiconductor unit can be mounted by processes other than lead bonding as, for example, by solder-bonding to the pads. Most preferably, these leads are formed from gold or include gold at their surfaces. Also, the semiconductor unit need not be an LED as discussed above with reference to FIG. **1**. Thus, the present invention can be applied to formation of an n-contact on any device which includes an n-type III–V region as discussed above.

As these and other variations and combinations of the features described above can be utilized without departing from the present invention, the foregoing description of the preferred embodiments should be taken by way of illustration rather than by way of limitation of the present invention.

What is claimed is:

1. A method of forming a contact on an n-type III–V semiconductor comprising the steps of:

(a) depositing Al on the n-type III–V semiconductor to provide a base layer; then

(b) depositing Ti on said base layer to provide a first barrier layer; then

(c) depositing Pt on said first barrier layer to provide a second barrier layer; then

(d) depositing Au on said second barrier layer to provide a top layer, whereby said base layer, said first barrier layer, said second barrier layer, and said top layer form a stack on the n-type semiconductor; and then

(e) annealing said n-type III–V semiconductor with said stack thereon.

2. A method as claimed in claim **1** wherein said annealing step is performed at about 400–600° C.

3. A method as claimed in, claim **2** wherein said annealing step is performed for between about 1 minute and about 10 minutes.

4. A method as claimed in claim **2** wherein said annealing step is performed for about 3 minutes.

5. A method as claimed in claim **4** wherein said annealing step is performed at about 500° C.

6. A method as claimed in claim **1** wherein said first barrier layer is at least about 300 Å thick.

7. A method as claimed in claim **6** wherein said first barrier layer is about 390 Å to about 410 Å thick.

8. A method as claimed in claim **6** wherein said deposited Al is between about 190 Å to about 210 Å thick.

9. A method as claimed in claim **6** wherein said second barrier layer is about 490 Å to about 510 Å thick.

10. A method as claimed in claim **6** wherein said top layer is at least about 6000 Å thick.

11. A method as claimed in claim **1** wherein said n-type semiconductor is a nitride compound semiconductor.

12. A method as claimed in claim **1** wherein said n-type semiconductor is a pure nitride compound semiconductor.

13. A method as claimed in claim **11** wherein said n-type semiconductor is a gallium nitride based semiconductor.

14. A method as claimed in claim **11** wherein said n-type semiconductor is GaN.

15. A method as claimed in claim **1** wherein said Al/Ti/Pt/Au contact has a contact resistance of less than about 10^{-5} ohm-cm^2.

16. A method as claimed in claim **1** wherein said base layer is about 20 nm thick.

17. A method as claimed in claim **1** wherein said base layer is less than about 50 nm thick.

* * * * *

United States Court of Appeals
for the Federal Circuit

CERTIFICATE OF SERVICE
Emcore Corporation v. Nichia Corporation, et al. No. 14-1508

I, Robyn Cocho, being duly sworn according to law and being over the age of 18, upon my oath depose and say that:

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On **August 27, 2014**, Counsel for Appellant has authorized me to electronically file the foregoing **Opening Brief of Appellant** with the Clerk of Court using the CM/ECF System, which will send notice of such filing to the following registered CM/ECF users:

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A courtesy copy will be sent to the above at the same time as copies are sent to the court.

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/s/Robyn Cocho
Counsel Press

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1. This brief complies with the type-volume limitation of Federal Rule of Appellate Procedure 32(a)(7)(B).

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2. This brief complies with the typeface requirements of Federal Rule of Appellate Procedure 32(a)(5) and the type style requirements of Federal Rule of Appellate Procedure 32(a)(6).

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